

## ISO724x High-Speed, Quad-Channel Digital Isolators

### 1 Features

- 25 and 150-Mbps Signaling Rate Options
  - Low Channel-to-Channel Output Skew; 1 ns Maximum
  - Low Pulse-Width Distortion (PWD); 2 ns Maximum
  - Low Jitter Content; 1 ns Typ at 150 Mbps
- Selectable Default Output (ISO7240CF)
- > 25-Year Life at Rated Working Voltage (see [High-Voltage Lifetime of the ISO72x Family of Digital Isolators](#) and [Isolation Capacitor Lifetime Projection](#))
- 4-kV ESD Protection
- Operates With 3.3-V or 5-V Supplies
- High Electromagnetic Immunity (see [ISO72x Digital Isolator Magnetic-Field Immunity](#))
- –40°C to +125°C Operating Temperature Range
- Safety-Related Certifications:
  - VDE 4000 V<sub>PK</sub> Basic Insulation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - 2.5 kV<sub>RMS</sub> Insulation for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A and IEC 60950-1 End Equipment Standard

### 2 Applications

- Industrial Fieldbus
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

### 3 Description

The ISO7240x, ISO7241x, and ISO7242x devices are quad-channel digital isolators with multiple channel configurations and output-enable functions. These devices have logic-input and logic-output buffers separated by Texas Instrument's silicon-dioxide (SiO<sub>2</sub>) isolation barrier. Used in conjunction with isolated power supplies, these devices help block high voltage, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

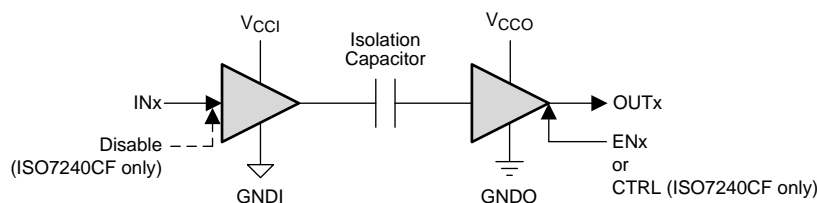
The ISO7240x family of devices has all four channels in the same direction. The ISO7241x family of devices has three channels in the same direction and one channel in the opposition direction. The ISO7242x family of devices has two channels in each direction.

Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE   | BODY SIZE (NOM)    |
|-------------|-----------|--------------------|
| ISO7240CF   | SOIC (16) | 10.30 mm x 7.50 mm |
| ISO7240C    |           |                    |
| ISO7240M    |           |                    |
| ISO7241C    |           |                    |
| ISO7241M    |           |                    |
| ISO7242C    |           |                    |
| ISO7242M    |           |                    |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Simplified Schematic



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V<sub>CCI</sub> and GNDI are supply and ground connections respectively for the input channels.

V<sub>CCO</sub> and GNDO are supply and ground connections respectively for the output channels.



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## 4 Revision History

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|---|------|
| • Added isolation resistance for $100^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ in the <i>Insulation Specifications</i> table..... | 11   |
| • Deleted the maximum transient overvoltage from VDE in the <i>Safety-Related Certifications</i> table.....                                 | 11   |
| • Added the <i>Receiving Notification of Documentation Updates</i> and the <i>Community Resources</i> section.....                          | 33   |

| Changes from Revision R (September 2015) to Revision S   | Page |
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| • Changed the HBM value from $\pm 4$ V to $\pm 4000$ V and the CDM value from $\pm 1$ V to $\pm 1000$ V in the <i>ESD Ratings</i> table.....         | 9    |
| • Moved the device power dissipation parameter from the <i>Thermal Information</i> table to the <i>Power Dissipation Characteristics</i> table ..... | 10   |

| Changes from Revision Q (January 2015) to Revision R   | Page |
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| • Changed <i>Features</i> From: "Basic Isolation per DIN EN 60747-5-5 (VDE 0884-5) & DIN EN 61010-1" To:"Basic Insulation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12" ..... | 1    |
| • Changed $V_{CC1}$ To $V_{CC1}$ , $V_{CC2}$ To $V_{CCO}$ , GND1 To GNDI, and GND2 To GNDO, and added Notes 1 and 2 to the   |      |

|  |    |
|--|----|
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| • Changed the CTI Test Conditions From: IEC 60112/VDE 0303 Part 1 To: DIN EN 60112 (VDE 0303-11); IEC 60112 in the <i>Package Characteristics</i> table .....  | 11 |
| • Changed section title From: <i>DIN EN 60747-5-5 Insulation Characteristics</i> To: <i>DIN V VDE V 0884-10 (VDE V 0884-10):2006-1 Insulation Characteristics</i> (.....   | 11 |
| • Deleted C <sub>1</sub> - Input capacitance to ground from the <i>Package Characteristics</i> table .....   | 11 |
| • Changed R <sub>S</sub> Test Conditions From: V <sub>IO</sub> = 500 V at T <sub>S</sub> To: V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C in the <i>DIN V VDE V 0884-10 (VDE V 0884-10):2006-1 Insulation Characteristics</i> table .....               | 11 |
| • Changed "DIN EN 60747-5-5 & DIN EN 61010-1" To: DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1): 2011-07 in the <i>Regulatory Information</i> table.....   | 11 |
| • Changed title From: <i>IEC Safety Limiting Values</i> To: <i>Safety Limiting Values</i> .....  | 12 |
| • Changed V <sub>OH</sub> MIN values From: V <sub>CC</sub> - 0.8 To: V <sub>CCO</sub> - 0.8 and V <sub>CC</sub> - 0.1 To: V <sub>CCO</sub> - 0.1 in the <i>Electrical Characteristics: V<sub>CC1</sub> and V<sub>CC2</sub> at 5-V Operation</i> .....        | 12 |
| • Changed V <sub>OH</sub> Test Condition ISO7240 To: 3.3-V side and the MIN value From: V <sub>CC</sub> - 0.4 To V <sub>CCO</sub> -0.4 in the <i>Electrical Characteristics: V<sub>CC1</sub> at 5-V, V<sub>CC2</sub> at 3.3-V Operation</i> .....            | 13 |
| • Changed V <sub>OH</sub> Test Condition ISO724x (5-V side) To: 5-V side and the MIN value From: V <sub>CC</sub> - 0.8 To: V <sub>CCO</sub> - 0.8 in the <i>Electrical Characteristics: V<sub>CC1</sub> at 5-V, V<sub>CC2</sub> at 3.3-V Operation</i> ..... | 13 |
| • Changed V <sub>OH</sub> , Test Condition I <sub>OH</sub> = -20 µA MIN value From: V <sub>CC</sub> - 0.1 To V <sub>CCO</sub> - 0.1 in the <i>lectrical Characteristics: VCC1 at 5-V, VCC2 at 3.3-V Operation</i> .....                                      | 13 |
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| • Changed V <sub>OH</sub> MIN values From: V <sub>CC</sub> - 0.4 To: V <sub>CCO</sub> - 0.4 and V <sub>CC</sub> - 0.1 To: V <sub>CCO</sub> - 0.1 in the <i>Electrical Characteristics: V<sub>CC1</sub> and V<sub>CC2</sub> at 3.3 V Operation</i> .....      | 15 |
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| • Changed V <sub>CC1</sub> To: V <sub>CC1</sub> and V <sub>CC2</sub> To: V <sub>CCO</sub> in Common-Mode Transient Immunity Test Circuit and Voltage Waveform ...  | 23 |

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| • Changed the V <sub>I</sub> MAX value in the <i>Absolute Maximum Ratings</i> table From: 6 V To: V <sub>CC</sub> + 0.5 V .....                         | 9  |
| • Added Note 3 to the <i>Absolute Maximum Ratings</i> table.....  | 9  |
| • Moved T <sub>STG</sub> - Storage From the <i>ESD Ratings</i> table to the <i>Absolute Maximum Ratings</i> table .....                                 | 9  |
| • Changed the <i>Handling Rating</i> table to the <i>ESD Ratings</i> table. ....  | 9  |
| • Added one row to the <i>ISO7240CF Functions Table</i> table. Values: X, PD, X, X, X, Undetermined .....   | 25 |
| • Added one row to the <i>Device Function Table ISO724x</i> table. Values: X, PD, X, X, Undetermined .....  | 25 |
| • Changed the <i>Device I/O Schematics</i> labels From: "ISO7240CF Input" To: "ISO7240CF Input, Disable" and From: "Enable" To: "Enable, Control" ..... | 26 |

**Changes from Revision O (November 2012) to Revision P**
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|--|---|
| • Added <i>Pin Configuration and Functions</i> section, <i>Handling Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | 1 |
| • Changed ISO7241C minimum supply from 2.8 V to 3.15 V .....   | 9 |

**Changes from Revision N (January 2012) to Revision O** **Page**

- Added the *Safety Limiting Values* section ..... 12

**Changes from Revision M (January 2011) to Revision N** **Page**

- Changed Feature From: Operates 3.3-V or 5-V Supplies To: Operates With 2.8-V (ISO7241C), 3.3-V or 5-V Supplies ..... 1
- Added device options to  $V_{CC}$  in the RECOMMENDED OPERATING CONDITIONS table ..... 9
- Changed Table Note (1) ..... 9
- Changed the CTI MIN value From:  $\geq 175$  V To:  $\geq 400$  V ..... 11
- Changed the *Regulatory Information* table ..... 11
- Changed Table Note (1) ..... 12
- Changed  $I_{CC1}$  and  $I_{CC2}$  test conditions in the  $V_{CC1}$  and  $V_{CC2}$  at 5-V *Electrical Characteristics:  $V_{CC1}$  and  $V_{CC2}$  at 5-V Operation* table ..... 12
- Changed Table Note (1) ..... 13
- Changed  $I_{CC1}$  and  $I_{CC2}$  test conditions in the  $V_{CC1}$  at 5-V,  $V_{CC2}$  at 3.3-V *Electrical Characteristics:  $V_{CC1}$  at 5-V,  $V_{CC2}$  at 3.3-V Operation* table ..... 13
- Changed Table Note (1) ..... 14
- Changed  $I_{CC1}$  and  $I_{CC2}$  test conditions in the  $V_{CC1}$  at 3.3-V,  $V_{CC2}$  at 5-V *Electrical Characteristics:  $V_{CC1}$  at 3.3-V,  $V_{CC2}$  at 5-V Operation* table ..... 14
- Changed Table Note (1) ..... 15
- Added ELECTRICAL and Switching CHARACTERISTICS tables for  $V_{CC1}$  and  $V_{CC2}$  at 2.8V (ISO722xC-only) ..... 15
- Changed  $I_{CC1}$  and  $I_{CC2}$  test conditions in the  $V_{CC1}$  and  $V_{CC2}$  at 3.3 V table ..... 15
- Changed  $V_{CC}$  *Undervoltage Threshold vs Free-Air Temperature* From  $V_{CC1}$  Failsafe Threshold To:  $V_{CC}$  Undervoltage Threshold ..... 19

**Changes from Revision L (January 2010) to Revision M** **Page**

- Changed the CSA File Number From: 1698195 To: 220991 ..... 11
- Changed Switching Characteristic Test Circuit and Voltage Waveforms, Failsafe Delay Time Test Circuit and Voltage Waveforms, and Wake Time From Input Disable Test Circuit and Voltage Waveforms ..... 21

**Changes from Revision K (December 2009) to Revision L** **Page**

- Added CTI - Tracking resistance (comparative tracking index to the *Package Characteristics* table ..... 11
- Added the IEC 60664-1 RATINGS TABLE ..... 11
- Added the IEC 60747-5-2 INSULATION CHARACTERISTIC table ..... 11

**Changes from Revision J (April 2009) to Revision K** **Page**

- Changed the Input circuit in the DEVICE I/O SCHEMATICS illustration ..... 1
- Added Note 1 to LI01), and changed the MIN value From: 8.34 To 8 mm in the *Package Characteristics* table ..... 11
- Added Note 1 to LI02), and changed the MIN value From: 8.1 To 8 mm in the *Package Characteristics* table ..... 11

**Changes from Revision I (December 2008) to Revision J** **Page**

- Changed  $I_{CC1}$  for Quiescent and 1Mbps From: 10mA To: 11mA ..... 12
- Changed  $I_{CC1}$  for Quiescent and 1Mbps From: 10mA To: 11mA ..... 13

| <b>Changes from Revision G (July 2008) to Revision H</b>   | <b>Page</b> |
|--|-------------|
| • Added Device number ISO7240CF.....   | 1           |
| • Added Features Bullet: Selectable Failsafe Output (ISO7240CF).....   | 1           |
| • Changed description paragraph 4 text.....  | 7           |
| • Changed $V_I$ in the <i>Absolute Maximum Ratings</i> table From: Voltage at IN, OUT, EN To: Voltage at IN, OUT, EN, DISABLE, CTRL..... | 9           |
| • Added $t_{wake}$ , Wake time from input disable.....   | 16          |
| • Added $t_{wake}$ , Wake time from input disable.....   | 16          |
| • Added $t_{wake}$ , Wake time from input disable.....   | 17          |
| • Added $t_{wake}$ , Wake time from input disable.....   | 17          |

| <b>Changes from Revision F (May 2008) to Revision G</b>  | <b>Page</b> |
|--|-------------|
| • Changed the <i>Package Characteristics</i> table, line , $L_{(IO1)}$ MIN value from 7.7mm to 8.34mm..... | 11          |

| <b>Changes from Revision E (May 2008) to Revision F</b>  | <b>Page</b> |
|--|-------------|
| • Deleted ISO724xA devices. See SLLS905 for the ISO7240A, ISO7241A, and ISO7242A.....  | 1           |
| • Changed Title From: QUAD DIGITAL ISOLATORS To: HIGH SPEED QUAD DIGITAL ISOLATORS.....  | 1           |
| • Changed Feature Low Jitter Content - From: 1, 25, and 150-Mbps Signaling Rate Options To: 25, and 150-Mbps Signaling Rate Options..... | 1           |
| • Added $t_{sk(pp)}$ footnote.....   | 16          |
| • Added $t_{sk(o)}$ footnote.....  | 16          |
| • Added $t_{sk(pp)}$ footnote.....   | 17          |
| • Added $t_{sk(o)}$ footnote.....  | 17          |

| <b>Changes from Revision D (April 2008) to Revision E</b>   | <b>Page</b> |
|---|-------------|
| • Added Table Note (1): For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V..... | 9           |
| • Added Table Note (1): For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V..... | 13          |
| • Added Table Note (1): For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V..... | 14          |
| • Added Table Note (1): For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V..... | 15          |

| <b>Changes from Revision C (April 2008) to Revision D</b>  | <b>Page</b> |
|--|-------------|
| • Added $t_{sk(pp)}$ Part-to-part skew.....  | 16          |
| • Added $t_{sk(pp)}$ Part-to-part skew.....  | 16          |
| • Added $t_{sk(pp)}$ Part-to-part skew.....  | 17          |
| • Added $t_{sk(pp)}$ Part-to-part skew.....  | 17          |
| • Changed Typical ISO724x Application Circuit, <i>Isolated Data Acquisition System for Process Control</i> ..... | 27          |

| <b>Changes from Revision B (August 2008) to Revision C</b>                     | <b>Page</b> |
|--|-------------|
| • Deleted Min = 4.5 V and max = 5.5 V for Supply Voltage of the ROC Table..... | 9           |
| • Changed $V_{CC}$ Supply Voltage in the ROC Table From: 3.6 To: 5.5.....      | 9           |

**Changes from Revision A (December 2007) to Revision B**

**Page**

- Changed  $V_{CC}$  Supply Voltage in the ROC Table From: 3.45 To: 3.6 ..... 9

**Changes from Original (September 2007) to Revision A**

**Page**

- Changed  $V_{CC}$  Supply Voltage in the ROC Table From: 3.6 To: 3.45 ..... 9
- Changed  $V_{CC}$  Supply Voltage in the ROC Table From: 3 To: 3.15 ..... 9
- Changed  $C_{IO}$  - typ value From: 1 To: 2 ..... 11
- Changed the *Regulatory Information*..... 11
- Changed  $C_1$  - typ value From: 1 To: 2 in the *Electrical Characteristics:  $V_{CC1}$  and  $V_{CC2}$  at 5-V Operation* ..... 12
- Changed TBDs to actual values. .... 12
- Changed  $C_1$  - typ value From: 1 To: 2 in the *Electrical Characteristics:  $V_{CC1}$  at 5-V,  $V_{CC2}$  at 3.3-V Operation*..... 13
- Changed  $C_1$  - typ value From: 1 To: 2 in the *Electrical Characteristics:  $V_{CC1}$  at 3.3-V,  $V_{CC2}$  at 5-V Operation*..... 14
- Changed typ value From: 1 To: 2 in the *Electrical Characteristics:  $V_{CC1}$  and  $V_{CC2}$  at 3.3 V Operation* ..... 15
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- Changed ISO724xA/C max value From: 3 To: 3.5..... 17
- Changed *ISO7240C/M RMS Supply Current vs Signaling Rate, ISO7241C/M RMS Supply Current vs Signaling Rate, and Propagation Delay vs Free-Air Temperature. Added ISO7242C/M RMS Supply Current vs Signaling Rate.* .... 19

## 5 Description (Continued)

The devices with the C suffix (C option) have TTL input thresholds and a noise-filter at the input that prevents transient pulses from being passed to the output of the device. The devices with the M suffix (M option) have CMOS  $V_{CC}/2$  input thresholds and do not have the input noise filter or the additional propagation delay.

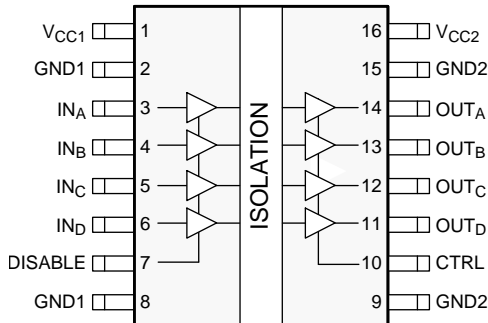
The ISO7240CF device has an input disable function on pin 7, and a selectable high or low failsafe-output function with the CTRL pin (pin 10). The failsafe output is a logic high when a logic high is placed on the CTRL pin or it is left unconnected. If a logic low signal is applied to the CTRL pin, the failsafe output becomes a logic-low output state. The input disable function of the ISO7240CF device prevents data from being passed across the isolation barrier to the output. When the inputs are disabled or  $V_{CC1}$  is powered down, the outputs are set by the CTRL pin.

These devices can be powered from 3.3-V or 5-V supplies on either side, in any combination. The signal input pins are 5-V tolerant regardless of the voltage supply level that is used.

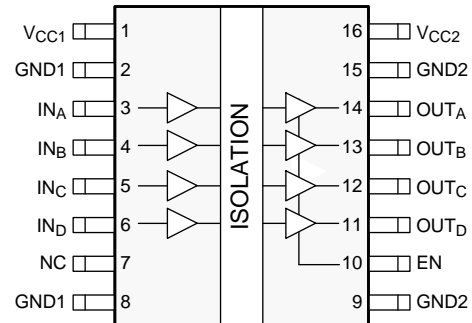
These devices are characterized for operation over the ambient temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

## 6 Pin Configurations and Functions

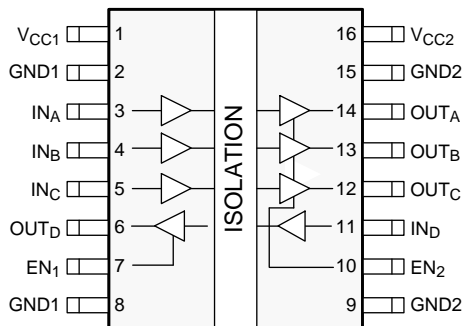
ISO7240CF DW Package  
 16-Pin SOIC  
 Top View



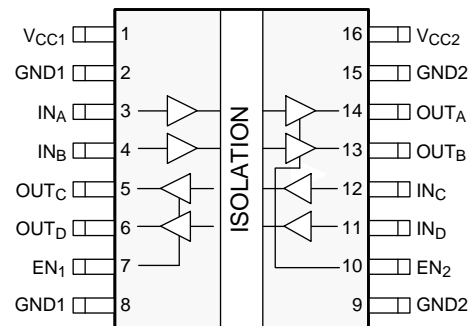
ISO7240C and ISO7240M DW Package  
 16-Pin SOIC  
 Top View



ISO7241C and ISO7241M DW Package  
 16-Pin SOIC  
 Top View



ISO7242C and ISO7242M DW Package  
 16-Pin SOIC  
 Top View



### Pin Functions

| NAME             | PIN NO.   |                      |                      |                      | I/O | DESCRIPTION <sup>3</sup>   |
|------------------|-----------|----------------------|----------------------|----------------------|-----|--|
|                  | ISO7240CF | ISO7240C<br>ISO7240M | ISO7241C<br>ISO7241M | ISO7242C<br>ISO7242M |     |  |
| CTRL             | 10        | —                    | —                    | —                    | I   | Failsafe output control. Output state is determined by CTRL pin when DISABLE is high or V <sub>CC1</sub> is powered down. Output is high when CTRL is high or open and low when CTRL is low. |
| DISABLE          | 7         | —                    | —                    | —                    | I   | Input disable. All input pins are disabled when DISABLE is high and enabled when DISABLE is low or open.   |
| EN               | —         | 10                   | —                    | —                    | I   | Output enable. All output pins are enabled when EN is high or open and disabled when EN is low.  |
| EN <sub>1</sub>  | —         | —                    | 7                    | 7                    | I   | Output enable 1. Output pins on side 1 are enabled when EN <sub>1</sub> is high or open and disabled when EN <sub>1</sub> is low.  |
| EN <sub>2</sub>  | —         | —                    | 10                   | 10                   | I   | Output enable 2. Output pins on side-2 are enabled when EN <sub>2</sub> is high or open and disabled when EN <sub>2</sub> is low.  |
| GND1             | 2, 8      | 2, 8                 | 2, 8                 | 2, 8                 | —   | Ground connection for V <sub>CC1</sub>   |
| GND2             | 9, 15     | 9, 15                | 9, 15                | 9, 15                | —   | Ground connection for V <sub>CC2</sub>   |
| IN <sub>A</sub>  | 3         | 3                    | 3                    | 3                    | I   | Input, channel A   |
| IN <sub>B</sub>  | 4         | 4                    | 4                    | 4                    | I   | Input, channel B   |
| IN <sub>C</sub>  | 5         | 5                    | 5                    | 12                   | I   | Input, channel C   |
| IN <sub>D</sub>  | 6         | 6                    | 11                   | 11                   | I   | Input, channel D   |
| NC               | —         | 7                    | —                    | —                    | —   | No Connect pins are floating with no internal connection   |
| OUT <sub>A</sub> | 14        | 14                   | 14                   | 14                   | O   | Output, channel A  |
| OUT <sub>B</sub> | 13        | 13                   | 13                   | 13                   | O   | Output, channel B  |
| OUT <sub>C</sub> | 12        | 12                   | 12                   | 5                    | O   | Output, channel C  |
| OUT <sub>D</sub> | 11        | 11                   | 6                    | 6                    | O   | Output, channel D  |
| V <sub>CC1</sub> | 1         | 1                    | 1                    | 1                    | —   | Power supply, V <sub>CC1</sub>   |
| V <sub>CC2</sub> | 16        | 16                   | 16                   | 16                   | —   | Power supply, V <sub>CC2</sub>   |



## 7 Specifications

### 7.1 Absolute Maximum Ratings

 See <sup>(1)</sup>

|           |   | MIN  | MAX                           | UNIT |
|-----------|---|------|-------------------------------|------|
| $V_{CC}$  | Supply voltage <sup>(2)</sup> , $V_{CC1}$ , $V_{CC2}$ | -0.5 | 6                             | V    |
| $V_I$     | Voltage at IN, OUT, EN, DISABLE, CTRL                 | -0.5 | $V_{CC} + 0.5$ <sup>(3)</sup> | V    |
| $I_O$     | Output current  | -15  | 15                            | mA   |
| $T_J$     | Maximum junction temperature                          |      | 170                           | °C   |
| $T_{stg}$ | Storage temperature                                   | -65  | 150                           | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal and are peak voltage values.
- (3) Maximum voltage must not exceed 6 V.

### 7.2 ESD Ratings

|             |                         | VALUE  | UNIT  |
|-------------|-------------------------|--|-------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±4000 |
|             |                         | Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |
|             |                         | Machine model (MM), per ANSI/ESDS5.2-1996                                      | ±200  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

|            |   | MIN      | NOM  | MAX                | UNIT |
|------------|---|----------|------|--------------------|------|
| $V_{CC}$   | Supply voltage <sup>(1)</sup> , $V_{CC1}$ , $V_{CC2}$                                       | 3.15     |      | 5.5                | V    |
| $I_{OH}$   | High-level output current   | -4       |      |                    | mA   |
| $I_{OL}$   | Low-level output current  |          |      | 4                  | mA   |
| $t_{ui}$   | Input pulse width   | ISO724xC | 40   |                    | ns   |
|            |   | ISO724xM | 6.67 | 5                  |      |
| $1/t_{ui}$ | Signaling rate  | ISO724xC | 0    | 30 <sup>(2)</sup>  | Mbps |
|            |   | ISO724xM | 0    | 200 <sup>(2)</sup> |      |
| $V_{IH}$   | High-level input voltage (IN)   |          |      | $V_{CC}$           | V    |
| $V_{IL}$   | Low-level input voltage (IN)  |          |      | $0.3 V_{CC}$       | V    |
| $V_{IH}$   | High-level input voltage (IN, DISABLE, CTRL, EN)  |          |      | 5.5                | V    |
| $V_{IL}$   | Low-level input voltage (IN, DISABLE, CTRL, EN)   |          |      | 0.8                | V    |
| $T_J$      | Junction temperature  |          |      | 150                | °C   |
| H          | External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification |          |      | 1000               | A/m  |

- (1) For the 5-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 4.5 V to 5.5 V.  
For the 3.3-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 3.15 V to 3.6 V.
- (2) Typical value at room temperature and well-regulated power supply.

## 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | ISO724xx     | UNIT |      |
|-------------------------------|--|--------------|------|------|
|                               |  | DW (SOIC)    |      |      |
|                               |  | 16 PINS      |      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | Low-K board  | 168  | °C/W |
|                               |  | High-K board | 77.3 | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    |              | 39.5 | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         |              | 41.9 | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   |              | 13.5 | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter |              | 41.9 | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance |              | n/a  | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Power Ratings

V<sub>CC1</sub> = V<sub>CC2</sub> = 5.5 V, T<sub>J</sub> = 150°C, C<sub>L</sub> = 15 pF, Input a 50% duty cycle square wave (unless otherwise noted)

| PARAMETER      | TEST CONDITIONS           | MIN | TYP | MAX | UNIT |
|----------------|---------------------------|-----|-----|-----|------|
| P <sub>D</sub> | Maximum power dissipation |     |     | 220 | mW   |

## 7.6 Insulation Specifications

| PARAMETER  |  | TEST CONDITIONS  | VALUE              | UNIT             |
|--|--|--|--------------------|------------------|
| <b>GENERAL</b>   |  |  |                    |                  |
| CLR  | External clearance <sup>(1)</sup>                    | Shortest terminal-to-terminal distance through air   | 8                  | mm               |
| CPG  | External creepage <sup>(1)</sup>                     | Shortest terminal-to-terminal distance across the package surface  | 8                  | mm               |
| DTI  | Distance through the insulation                      | Minimum internal gap (internal clearance)  | 0.008              | mm               |
| CTI  | Comparative tracking index                           | DIN EN 60112 (VDE 0303-11); IEC 60112  | ≥ 400              | V                |
|  | Material group                                       |  | II                 |                  |
|  | Overvoltage Category                                 | Rated mains voltage ≤ 150 V <sub>RMS</sub>   | I-IV               |                  |
|  |  | Rated mains voltage ≤ 300 V <sub>RMS</sub>   | I-III              |                  |
| <b>DIN V VDE V 0884-10 (VDE V 0884-10):2006-12<sup>(2)</sup></b> |  |  |                    |                  |
| V <sub>IORM</sub>  | Maximum repetitive peak isolation voltage            | AC voltage (bipolar)   | 560                | V <sub>PK</sub>  |
| V <sub>IOTM</sub>  | Maximum transient isolation voltage                  | V <sub>TEST</sub> = V <sub>IOTM</sub><br>t = 60 s (qualification), t = 1 s (100% production)   | 4000               | V <sub>PK</sub>  |
| q <sub>pd</sub>  | Apparent charge <sup>(3)</sup>                       | Method a: After I/O safety test subgroup 2/3.<br>V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s;<br>V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s,                              | ≤ 5                | pC               |
|  |  | Method a: After environmental tests subgroup 1,<br>V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s;<br>V <sub>pd(m)</sub> = 1.3 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s,                            | ≤ 5                |                  |
|  |  | Method b1: At routine test (100% production) and preconditioning (type test)<br>V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s;<br>V <sub>pd(m)</sub> = 1.5 × V <sub>IORM</sub> , t <sub>m</sub> = 1 s, | ≤ 5                |                  |
| C <sub>IO</sub>  | Barrier capacitance, input to output <sup>(4)</sup>  | V <sub>I</sub> = 0.4 sin (4E6πt)   | 2                  | pF               |
| R <sub>IO</sub>  | Isolation resistance, input to output <sup>(4)</sup> | V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C   | > 10 <sup>12</sup> | Ω                |
|  |  | V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 125°C  | > 10 <sup>11</sup> |                  |
|  |  | V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C  | > 10 <sup>9</sup>  |                  |
|  | Pollution degree                                     |  | 2                  |                  |
|  | Climatic category                                    |  | 40/125/21          |                  |
| <b>UL 1577</b>   |  |  |                    |                  |
| V <sub>ISO</sub>   | Withstand isolation voltage                          | V <sub>TEST</sub> = V <sub>ISO</sub> = 2500 V <sub>RMS</sub> , t = 60 s (qualification);<br>V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> = 3000 V <sub>RMS</sub> , t = 1 s (100% production)                             | 2500               | V <sub>RMS</sub> |

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (4) All pins on each side of the barrier tied together creating a two-terminal device

## 7.7 Safety-Related Certifications

| VDE   | CSA   | UL   |
|---|---|--|
| Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1): 2011-07                                       | Approved under CSA Component Acceptance Notice 5A and IEC 60950-1   | Recognized under UL 1577 Component Recognition Program |
| Basic Insulation<br>Maximum Transient Isolation Voltage, 4000 V <sub>PK</sub> ;<br>Maximum Repetitive Peak Isolation Voltage, 560 V <sub>PK</sub> | 4000 V <sub>PK</sub> maximum isolation rating;<br>Basic insulation per CSA 60950-1-07 and IEC 60950-1 (2nd Ed), 366 V <sub>RMS</sub> maximum working voltage, | Single protection, 2500 V <sub>RMS</sub>               |
| Certificate Number: 40016131  | Master Contract Number: 220991  | File Number: E181974                                   |

## 7.8 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

| PARAMETER  | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|--|---|-----|-----|-----|------|
| I <sub>S</sub> Safety input, output, or supply current | R <sub>θJA</sub> = 168°C/W, V <sub>I</sub> = 5.5 V, T <sub>J</sub> = 170°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 2</a> |     |     | 156 | mA   |
|  | R <sub>θJA</sub> = 168°C/W, V <sub>I</sub> = 3.6 V, T <sub>J</sub> = 170°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 2</a> |     |     | 239 |      |
| T <sub>S</sub> Safety temperature                      |   |     |     | 150 | °C   |

- (1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

## 7.9 Electrical Characteristics: V<sub>CC1</sub> and V<sub>CC2</sub> at 5-V Operation

For the 5-V operation, V<sub>CC1</sub> or V<sub>CC2</sub> is specified from 4.5 V to 5.5 V. Over recommended operating conditions (unless otherwise noted)

| PARAMETER                                    | TEST CONDITIONS  | MIN                    | TYP | MAX | UNIT  |
|--|--|------------------------|-----|-----|-------|
| I <sub>OFF</sub> Sleep mode output current   | EN at 0 V, Single channel  |                        | 0   |     | μA    |
| V <sub>OH</sub> High-level output voltage    | I <sub>OH</sub> = -4 mA, See <a href="#">Figure 11</a>                 | V <sub>CC0</sub> - 0.8 |     |     | V     |
|  | I <sub>OH</sub> = -20 μA, See <a href="#">Figure 11</a>                | V <sub>CC0</sub> - 0.1 |     |     |       |
| V <sub>OL</sub> Low-level output voltage     | I <sub>OL</sub> = 4 mA, See <a href="#">Figure 11</a>                  |                        |     | 0.4 | V     |
|  | I <sub>OL</sub> = 20 μA, See <a href="#">Figure 11</a>                 |                        |     | 0.1 |       |
| V <sub>I(HYS)</sub> Input voltage hysteresis |  |                        | 150 |     | mV    |
| I <sub>IH</sub> High-level input current     | IN at V <sub>CC1</sub>   |                        |     | 10  | μA    |
| I <sub>IL</sub> Low-level input current      | IN at 0 V  | -10                    |     |     |       |
| C <sub>I</sub> Input capacitance to ground   | IN at V <sub>CC</sub> , V <sub>I</sub> = 0.4 sin(4E6πt)                |                        | 2   |     | pF    |
| CMTI Common-mode transient immunity          | V <sub>I</sub> = V <sub>CC</sub> or 0 V, See <a href="#">Figure 15</a> | 25                     | 50  |     | kV/μs |

## 7.10 Supply Current Characteristics: V<sub>CC1</sub> and V<sub>CC2</sub> at 5-V Operation

For the 5-V operation, V<sub>CC1</sub> or V<sub>CC2</sub> is specified from 4.5 V to 5.5 V. Over recommended operating conditions (unless otherwise noted)

| PARAMETER                               | TEST CONDITIONS  | MIN | TYP | MAX  | UNIT |
|---|--|-----|-----|------|------|
| <b>ISO7240C/M</b>                       |  |     |     |      |      |
| I <sub>CC1</sub> Supply current, side 1 | Quiescent, All channels, no load, EN at 3 V, V <sub>I</sub> = V <sub>CC</sub> or 0 V |     | 1   | 3    | mA   |
|   | 25 Mbps, All channels, no load, EN at 3 V, 12.5-MHz input-clock signal               |     | 7   | 10.5 |      |
| I <sub>CC2</sub> Supply current, side 2 | All channels, no load, EN at 3 V   |     | 15  | 22   | mA   |
|   | 25 Mbps, 12.5-MHz input-clock signal   |     | 17  | 25   |      |
| <b>ISO7241C/M</b>                       |  |     |     |      |      |
| I <sub>CC1</sub> Supply current, side 1 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V                |     | 6.5 | 11   | mA   |
|   | 25 Mbps, 12.5-MHz input-clock signal   |     | 12  | 18   |      |
| I <sub>CC2</sub> Supply current, side 2 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V                |     | 13  | 20   | mA   |
|   | 25 Mbps, 12.5-MHz input-clock signal   |     | 18  | 28   |      |
| <b>ISO7242C/M</b>                       |  |     |     |      |      |
| I <sub>CC1</sub> Supply current, side 1 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V                |     | 10  | 16   | mA   |
|   | 25 Mbps, 12.5-MHz input-clock signal   |     | 15  | 24   |      |
| I <sub>CC2</sub> Supply current, side 2 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V                |     | 10  | 16   | mA   |
|   | 25 Mbps, 12.5-MHz input-clock signal   |     | 15  | 24   |      |

### 7.11 Electrical Characteristics: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V Operation

For the 5-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 4.5 V to 5.5 V. For the 3.3-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

| PARAMETER    |                                | TEST CONDITIONS                                       |            | MIN             | TYP | MAX | UNIT        |
|--------------|--------------------------------|---|------------|-----------------|-----|-----|-------------|
| $I_{OFF}$    | Sleep mode output current      | EN at 0 V, Single channel                             |            |                 | 0   |     | $\mu$ A     |
| $V_{OH}$     | High-level output voltage      | $I_{OH} = -4$ mA, See <a href="#">Figure 11</a>       | 3.3-V side | $V_{CCO} - 0.4$ |     |     | V           |
|              |                                |   | 5-V side   | $V_{CCO} - 0.8$ |     |     |             |
|              |                                | $I_{OH} = -20$ $\mu$ A, See <a href="#">Figure 11</a> |            | $V_{CCO} - 0.1$ |     |     |             |
| $V_{OL}$     | Low-level output voltage       | $I_{OL} = 4$ mA, See <a href="#">Figure 11</a>        |            |                 |     | 0.4 | V           |
|              |                                | $I_{OL} = 20$ $\mu$ A, See <a href="#">Figure 11</a>  |            |                 |     | 0.1 |             |
| $V_{I(HYS)}$ | Input voltage hysteresis       |   |            |                 | 150 |     | mV          |
| $I_{IH}$     | High-level input current       | IN at $V_{CC1}$                                       |            |                 |     | 10  | $\mu$ A     |
| $I_{IL}$     | Low-level input current        | IN at 0 V   |            | -10             |     |     |             |
| $C_1$        | Input capacitance to ground    | IN at $V_{CC}$ , $V_I = 0.4 \sin(4E6\pi t)$           |            |                 | 2   |     | pF          |
| CMTI         | Common-mode transient immunity | $V_I = V_{CC}$ or 0 V, See <a href="#">Figure 15</a>  |            | 25              | 50  |     | kV/ $\mu$ s |

### 7.12 Supply Current Characteristics: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V Operation

For the 5-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 4.5 V to 5.5 V. For the 3.3-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

| PARAMETER         |                        | TEST CONDITIONS   |                                      | MIN | TYP  | MAX  | UNIT |
|-------------------|------------------------|---|--------------------------------------|-----|------|------|------|
| <b>ISO7240C/M</b> |                        |   |                                      |     |      |      |      |
| $I_{CC1}$         | Supply current, side 1 | All channels, no load, EN at 3 V                                      | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 1    | 3    | mA   |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 7    | 10.5 |      |
| $I_{CC2}$         | Supply current, side 2 | All channels, no load, EN at 3 V                                      | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 9.5  | 15   | mA   |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 10.5 | 17   |      |
| <b>ISO7241C/M</b> |                        |   |                                      |     |      |      |      |
| $I_{CC1}$         | Supply current, side 1 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 6.5  | 11   | mA   |
|                   |                        |   | 12.5-MHz input-clock signal          |     | 12   | 18   |      |
| $I_{CC2}$         | Supply current, side 2 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 8    | 13   | mA   |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 11.5 | 18   |      |
| <b>ISO7242C/M</b> |                        |   |                                      |     |      |      |      |
| $I_{CC1}$         | Supply current, side 1 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 10   | 16   | mA   |
|                   |                        |   | 12.5-MHz input-clock signal          |     | 15   | 24   |      |
| $I_{CC2}$         | Supply current, side 2 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 6    | 10   | mA   |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 9    | 14   |      |

### 7.13 Electrical Characteristics: $V_{CC1}$ at 3.3-V, $V_{CC2}$ at 5-V Operation

For the 5-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 4.5 V to 5.5 V. For the 3.3-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

| PARAMETER    |                                | TEST CONDITIONS                                       |            | MIN             | TYP | MAX | UNIT        |
|--------------|--------------------------------|---|------------|-----------------|-----|-----|-------------|
| $I_{OFF}$    | Sleep mode output current      | EN at 0 V, Single channel                             |            |                 | 0   |     | $\mu$ A     |
| $V_{OH}$     | High-level output voltage      | $I_{OH} = -4$ mA, See <a href="#">Figure 11</a>       | 3.3-V side | $V_{CCO} - 0.4$ |     |     | V           |
|              |                                |   | 5-V side   | $V_{CCO} - 0.8$ |     |     |             |
|              |                                | $I_{OH} = -20$ $\mu$ A, See <a href="#">Figure 11</a> |            | $V_{CCO} - 0.1$ |     |     |             |
| $V_{OL}$     | Low-level output voltage       | $I_{OL} = 4$ mA, See <a href="#">Figure 11</a>        |            |                 |     | 0.4 | V           |
|              |                                | $I_{OL} = 20$ $\mu$ A, See <a href="#">Figure 11</a>  |            |                 |     | 0.1 |             |
| $V_{I(HYS)}$ | Input voltage hysteresis       |   |            |                 | 150 |     | mV          |
| $I_{IH}$     | High-level input current       | IN at $V_{CC1}$                                       |            |                 |     | 10  | $\mu$ A     |
| $I_{IL}$     | Low-level input current        | IN at 0 V   |            | -10             |     |     |             |
| $C_1$        | Input capacitance to ground    | IN at $V_{CC}$ , $V_I = 0.4 \sin(4E6\pi t)$           |            |                 | 2   |     | pF          |
| CMTI         | Common-mode transient immunity | $V_I = V_{CC}$ or 0 V, See <a href="#">Figure 15</a>  |            | 25              | 50  |     | kV/ $\mu$ s |

### 7.14 Supply Current Characteristics: $V_{CC1}$ at 3.3-V, $V_{CC2}$ at 5-V Operation

For the 5-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 4.5 V to 5.5 V. For the 3.3-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

| PARAMETER         |                        | TEST CONDITIONS   |                                      | MIN | TYP | MAX | UNIT |
|-------------------|------------------------|---|--------------------------------------|-----|-----|-----|------|
| <b>ISO7240C/M</b> |                        |   |                                      |     |     |     |      |
| $I_{CC1}$         | Supply current, side 1 | All channels, no load, EN at 3 V                                      | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 0.5 | 1   | mA   |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 3   | 5   |      |
| $I_{CC2}$         | Supply current, side 2 | All channels, no load, EN at 3 V                                      | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 15  | 22  | mA   |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 17  | 25  |      |
| <b>ISO7241C/M</b> |                        |   |                                      |     |     |     |      |
| $I_{CC1}$         | Supply current, side 1 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 4   | 7   | mA   |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 6.5 | 11  |      |
| $I_{CC2}$         | Supply current, side 2 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 13  | 20  | mA   |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 18  | 28  |      |
| <b>ISO7242C/M</b> |                        |   |                                      |     |     |     |      |
| $I_{CC1}$         | Supply current, side 1 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 6   | 10  | mA   |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 9   | 14  |      |
| $I_{CC2}$         | Supply current, side 2 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 10  | 16  | mA   |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 15  | 24  |      |

## 7.15 Electrical Characteristics: $V_{CC1}$ and $V_{CC2}$ at 3.3 V Operation

For the 3.3-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

| PARAMETER    |                                | TEST CONDITIONS                                       | MIN             | TYP | MAX | UNIT        |
|--------------|--------------------------------|---|-----------------|-----|-----|-------------|
| $I_{OFF}$    | Sleep mode output current      | EN at 0 V, single channel                             |                 | 0   |     | $\mu$ A     |
| $V_{OH}$     | High-level output voltage      | $I_{OH} = -4$ mA, See <a href="#">Figure 11</a>       | $V_{CCO} - 0.4$ |     |     | V           |
|              |                                | $I_{OH} = -20$ $\mu$ A, See <a href="#">Figure 11</a> | $V_{CCO} - 0.1$ |     |     |             |
| $V_{OL}$     | Low-level output voltage       | $I_{OL} = 4$ mA, See <a href="#">Figure 11</a>        |                 |     | 0.4 | V           |
|              |                                | $I_{OL} = 20$ $\mu$ A, See <a href="#">Figure 11</a>  |                 |     | 0.1 |             |
| $V_{I(HYS)}$ | Input voltage hysteresis       |   |                 | 150 |     | mV          |
| $I_{IH}$     | High-level input current       | IN at $V_{CCI}$                                       |                 |     | 10  | $\mu$ A     |
| $I_{IL}$     | Low-level input current        | IN at 0 V   | -10             |     |     |             |
| $C_I$        | Input capacitance to ground    | IN at $V_{CC}$ , $V_I = 0.4 \sin(4E6\pi t)$           |                 | 2   |     | pF          |
| CMTI         | Common-mode transient immunity | $V_I = V_{CC}$ or 0 V, See <a href="#">Figure 15</a>  | 25              | 50  |     | kV/ $\mu$ s |

## 7.16 Supply Current Characteristics: $V_{CC1}$ and $V_{CC2}$ at 3.3 V Operation

For the 3.3-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

| PARAMETER         |                        | TEST CONDITIONS   | MIN                                  | TYP | MAX  | UNIT |    |
|-------------------|------------------------|---|--------------------------------------|-----|------|------|----|
| <b>ISO7240C/M</b> |                        |   |                                      |     |      |      |    |
| $I_{CC1}$         | Supply current, side 1 | All channels, no load, EN at 3 V                                      | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 0.5  | 1    | mA |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 3    | 5    |    |
| $I_{CC2}$         | Supply current, side 2 | All channels, no load, EN at 3 V                                      | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 9.5  | 15   | mA |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 10.5 | 17   |    |
| <b>ISO7241C/M</b> |                        |   |                                      |     |      |      |    |
| $I_{CC1}$         | Supply current, side 1 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 4    | 7    | mA |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 6.5  | 11   |    |
| $I_{CC2}$         | Supply current, side 2 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 8    | 13   | mA |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 11.5 | 18   |    |
| <b>ISO7242C/M</b> |                        |   |                                      |     |      |      |    |
| $I_{CC1}$         | Supply current, side 1 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 6    | 10   | mA |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 9    | 14   |    |
| $I_{CC2}$         | Supply current, side 2 | All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V | Quiescent, $V_I = V_{CC}$ or 0 V     |     | 6    | 10   | mA |
|                   |                        |   | 25 Mbps, 12.5-MHz input-clock signal |     | 9    | 14   |    |

## 7.17 Switching Characteristics: $V_{CC1}$ and $V_{CC2}$ at 5-V Operation

over recommended operating conditions (unless otherwise noted)

| PARAMETER             |   | TEST CONDITIONS           | MIN   | TYP | MAX | UNIT    |    |
|-----------------------|---|---------------------------|---|-----|-----|---------|----|
| $t_{PLH}$ , $t_{PHL}$ | Propagation delay   | ISO724xC<br>See Figure 11 | 18  |     | 42  | ns      |    |
| PWD                   | Pulse-width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $ |                           |   |     | 2.5 |         |    |
| $t_{PLH}$ , $t_{PHL}$ | Propagation delay   | ISO724xM                  | 10  |     | 23  | ns      |    |
| PWD                   | Pulse-width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $ |                           |   |     | 1   |         | 2  |
| $t_{sk(pp)}$          | Part-to-part skew <sup>(2)</sup>                            | ISO724xC                  |   |     | 8   | ns      |    |
|                       |   | ISO724xM                  |   |     | 0   |         | 3  |
| $t_{sk(o)}$           | Channel-to-channel output skew <sup>(3)</sup>               | ISO724xC                  |   |     | 2   | ns      |    |
|                       |   | ISO724xM                  |   |     | 0   |         | 1  |
| $t_r$                 | Output signal rise time                                     | See Figure 11             |   |     | 2   | ns      |    |
| $t_f$                 | Output signal fall time                                     |                           |   |     | 2   |         |    |
| $t_{PHZ}$             | Propagation delay, high-level-to-high-impedance output      | See Figure 12             |   |     | 15  | 20      | ns |
| $t_{PZH}$             | Propagation delay, high-impedance-to-high-level output      |                           |   |     | 15  | 20      |    |
| $t_{PLZ}$             | Propagation delay, low-level-to-high-impedance output       |                           |   |     | 15  | 20      |    |
| $t_{PZL}$             | Propagation delay, high-impedance-to-low-level output       |                           |   |     | 15  | 20      |    |
| $t_{fs}$              | Failsafe output delay time from input power loss            | See Figure 13             |   |     | 12  | $\mu$ s |    |
| $t_{wake}$            | Wake time from input disable                                | See Figure 14             |   |     | 15  | $\mu$ s |    |
| $t_{jit(pp)}$         | Peak-to-peak eye-pattern jitter                             | ISO724xM                  | 150 Mbps NRZ data input, Same polarity input on all channels, See Figure 16 |     | 1   | ns      |    |

- (1) Also referred to as pulse skew.
- (2)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- (3)  $t_{sk(o)}$  is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

## 7.18 Switching Characteristics: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

| PARAMETER             |   | TEST CONDITIONS           | MIN  | TYP | MAX | UNIT    |    |
|-----------------------|---|---------------------------|--|-----|-----|---------|----|
| $t_{PLH}$ , $t_{PHL}$ | Propagation delay   | ISO724xC<br>See Figure 11 | 20   |     | 50  | ns      |    |
| PWD                   | Pulse-width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $ |                           |  |     | 3   |         |    |
| $t_{PLH}$ , $t_{PHL}$ | Propagation delay   | ISO724xM                  | 12   |     | 29  | ns      |    |
| PWD                   | Pulse-width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $ |                           |  |     | 1   |         | 2  |
| $t_{sk(pp)}$          | Part-to-part skew <sup>(2)</sup>                            | ISO724xC                  |  |     | 10  | ns      |    |
|                       |   | ISO724xM                  |  |     | 0   |         | 5  |
| $t_{sk(o)}$           | Channel-to-channel output skew <sup>(3)</sup>               | ISO724xC                  |  |     | 3   | ns      |    |
|                       |   | ISO724xM                  |  |     | 0   |         | 1  |
| $t_r$                 | Output signal rise time                                     | See Figure 11             |  |     | 2   | ns      |    |
| $t_f$                 | Output signal fall time                                     |                           |  |     | 2   |         |    |
| $t_{PHZ}$             | Propagation delay, high-level-to-high-impedance output      | See Figure 12             |  |     | 15  | 20      | ns |
| $t_{PZH}$             | Propagation delay, high-impedance-to-high-level output      |                           |  |     | 15  | 20      |    |
| $t_{PLZ}$             | Propagation delay, low-level-to-high-impedance output       |                           |  |     | 15  | 20      |    |
| $t_{PZL}$             | Propagation delay, high-impedance-to-low-level output       |                           |  |     | 15  | 20      |    |
| $t_{fs}$              | Failsafe output delay time from input power loss            | See Figure 13             |  |     | 18  | $\mu$ s |    |
| $t_{wake}$            | Wake time from input disable                                | See Figure 14             |  |     | 15  | $\mu$ s |    |
| $t_{jit(pp)}$         | Peak-to-peak eye-pattern jitter                             | ISO724xM                  | 150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 16 |     | 1   | ns      |    |

- (1) Also known as pulse skew
- (2)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- (3)  $t_{sk(o)}$  is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.



## 7.19 Switching Characteristics: $V_{CC1}$ at 3.3-V and $V_{CC2}$ at 5-V Operation

over recommended operating conditions (unless otherwise noted)

| PARAMETER             |   |          | TEST CONDITIONS   | MIN      | TYP           | MAX | UNIT    |
|-----------------------|---|----------|---|----------|---------------|-----|---------|
| $t_{PLH}$ , $t_{PHL}$ | Propagation delay   |          |   | ISO724xC | See Figure 11 | 22  |         |
| PWD                   | Pulse-width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $ |          |   |          |               | 3   |         |
| $t_{PLH}$ , $t_{PHL}$ | Propagation delay   | ISO724xM | 12  |          |               | 30  | ns      |
| PWD                   | Pulse-width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $ |          |   | 1        |               | 2   |         |
| $t_{sk(pp)}$          | Part-to-part skew <sup>(2)</sup>                            | ISO724xC |   |          | 10            | ns  |         |
|                       |   | ISO724xM |   | 0        | 5             |     |         |
| $t_{sk(o)}$           | Channel-to-channel output skew <sup>(3)</sup>               | ISO724xC |   |          | 2.5           | ns  |         |
|                       |   | ISO724xM |   | 0        | 1             |     |         |
| $t_r$                 | Output signal rise time                                     |          | See Figure 11   |          | 2             |     | ns      |
| $t_f$                 | Output signal fall time                                     |          |   |          | 2             |     |         |
| $t_{PHZ}$             | Propagation delay, high-level-to-high-impedance output      |          | See Figure 12   |          | 15            | 20  | ns      |
| $t_{PZH}$             | Propagation delay, high-impedance-to-high-level output      |          |   |          | 15            | 20  |         |
| $t_{PLZ}$             | Propagation delay, low-level-to-high-impedance output       |          |   |          | 15            | 20  |         |
| $t_{PZL}$             | Propagation delay, high-impedance-to-low-level output       |          |   |          | 15            | 20  |         |
| $t_{fs}$              | Failsafe output delay time from input power loss            |          | See Figure 13   |          | 12            |     | $\mu$ s |
| $t_{wake}$            | Wake time from input disable                                |          | See Figure 14   |          | 15            |     | $\mu$ s |
| $t_{jit(pp)}$         | Peak-to-peak eye-pattern jitter                             | ISO724xM | 150 Mbps NRZ data input, Same polarity input on all channels, See Figure 16 |          | 1             |     | ns      |

(1) Also known as pulse skew

(2)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3)  $t_{sk(o)}$  is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

## 7.20 Switching Characteristics: $V_{CC1}$ and $V_{CC2}$ at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

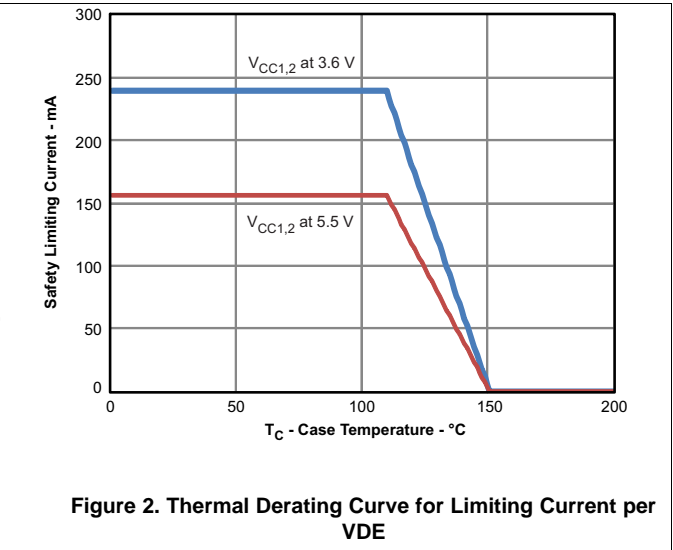
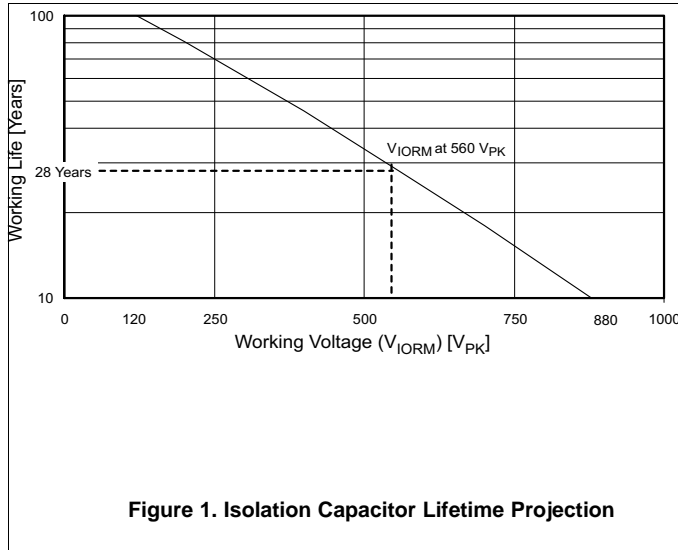
| PARAMETER             |   |          | TEST CONDITIONS  | MIN      | TYP           | MAX | UNIT    |
|-----------------------|---|----------|--|----------|---------------|-----|---------|
| $t_{PLH}$ , $t_{PHL}$ | Propagation delay   |          |  | ISO724xC | See Figure 11 | 25  |         |
| PWD                   | Pulse-width distortion $ t_{PHL} - t_{PLH} $ <sup>(1)</sup> |          |  |          |               | 4   |         |
| $t_{PLH}$ , $t_{PHL}$ | Propagation delay   | ISO724xM | 12   |          |               | 34  | ns      |
| PWD                   | Pulse-width distortion $ t_{PHL} - t_{PLH} $ <sup>(1)</sup> |          |  | 1        |               | 2   |         |
| $t_{sk(pp)}$          | Part-to-part skew <sup>(2)</sup>                            | ISO724xC |  |          | 10            | ns  |         |
|                       |   | ISO724xM |  | 0        | 5             |     |         |
| $t_{sk(o)}$           | Channel-to-channel output skew <sup>(3)</sup>               | ISO724xC |  |          | 3.5           | ns  |         |
|                       |   | ISO724xM |  | 0        | 1             |     |         |
| $t_r$                 | Output signal rise time                                     |          | See Figure 11  |          | 2             |     | ns      |
| $t_f$                 | Output signal fall time                                     |          |  |          | 2             |     |         |
| $t_{PHZ}$             | Propagation delay, high-level-to-high-impedance output      |          | See Figure 12  |          | 15            | 20  | ns      |
| $t_{PZH}$             | Propagation delay, high-impedance-to-high-level output      |          |  |          | 15            | 20  |         |
| $t_{PLZ}$             | Propagation delay, low-level-to-high-impedance output       |          |  |          | 15            | 20  |         |
| $t_{PZL}$             | Propagation delay, high-impedance-to-low-level output       |          |  |          | 15            | 20  |         |
| $t_{fs}$              | Failsafe output delay time from input power loss            |          | See Figure 13  |          | 18            |     | $\mu$ s |
| $t_{wake}$            | Wake time from input disable                                |          | See Figure 14  |          | 15            |     | $\mu$ s |
| $t_{jit(pp)}$         | Peak-to-peak eye-pattern jitter                             | ISO724xM | 150 Mbps PRBS NRZ data input, same polarity input on all channels, See Figure 16 |          | 1             |     | ns      |

(1) Also referred to as pulse skew.

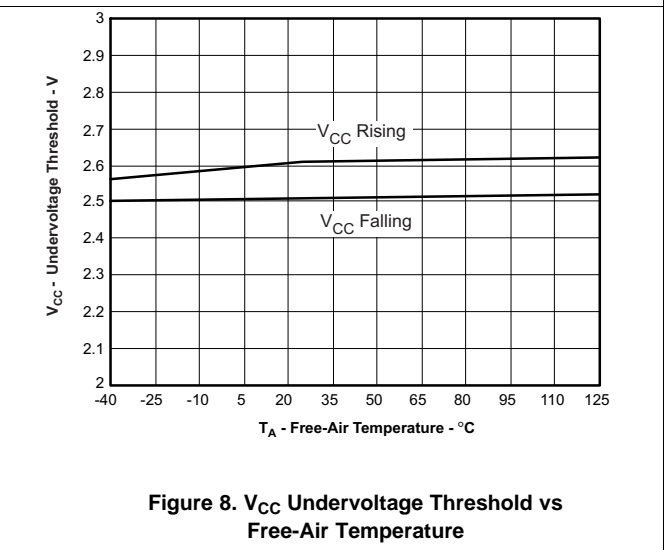
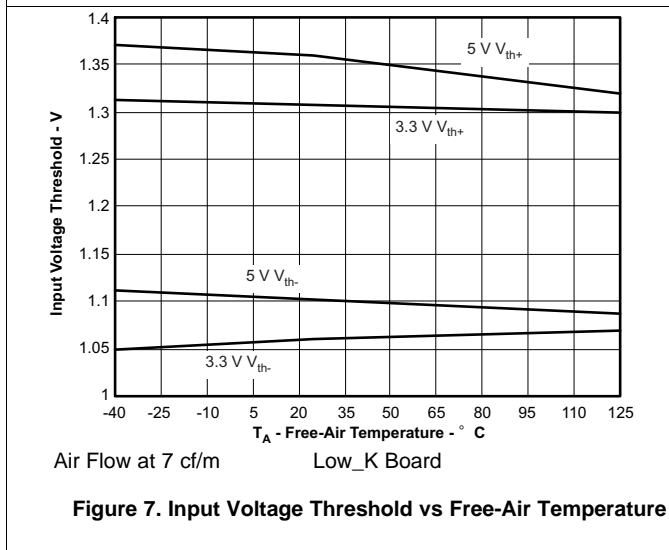
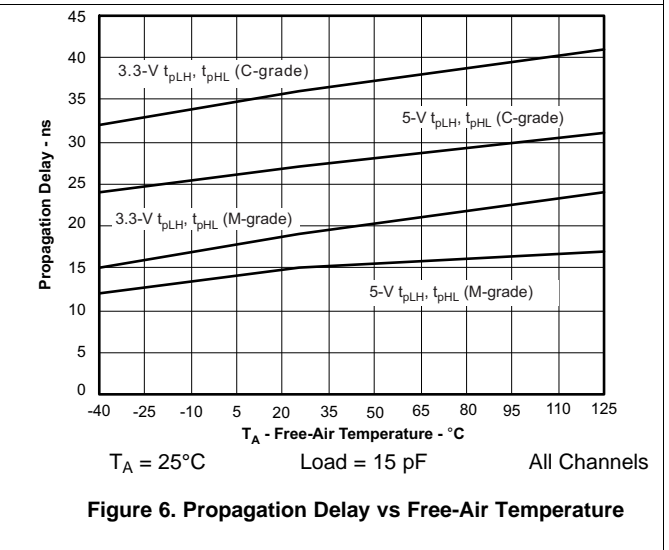
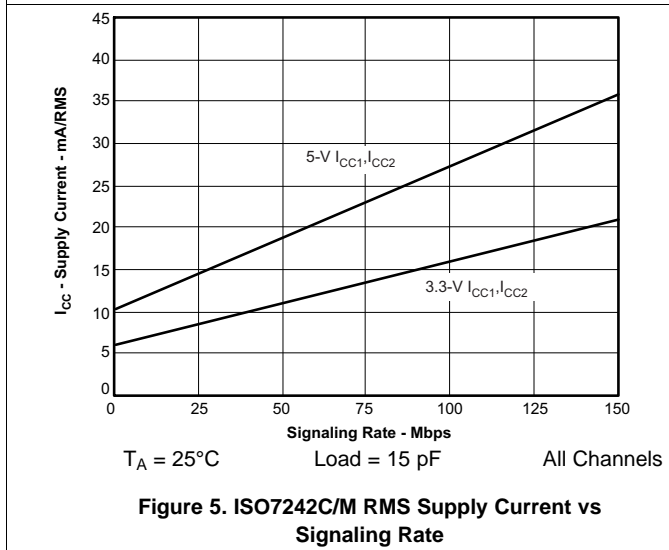
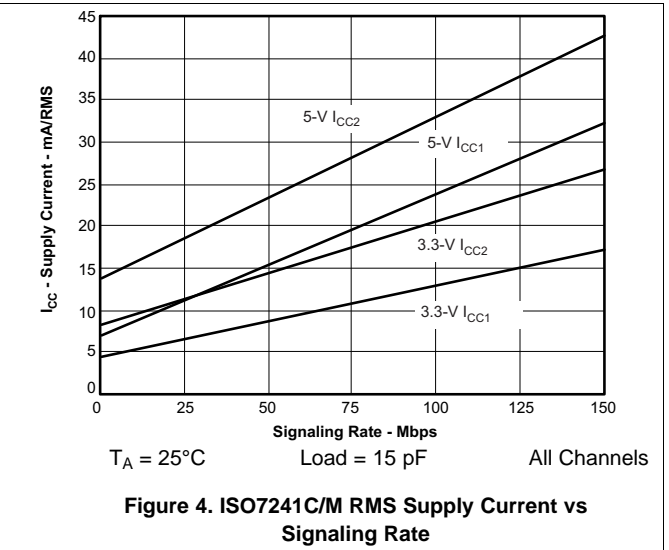
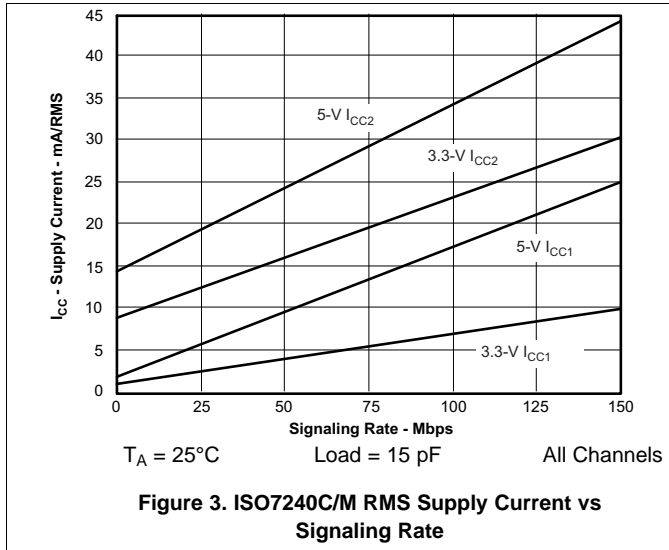
(2)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3)  $t_{sk(o)}$  is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

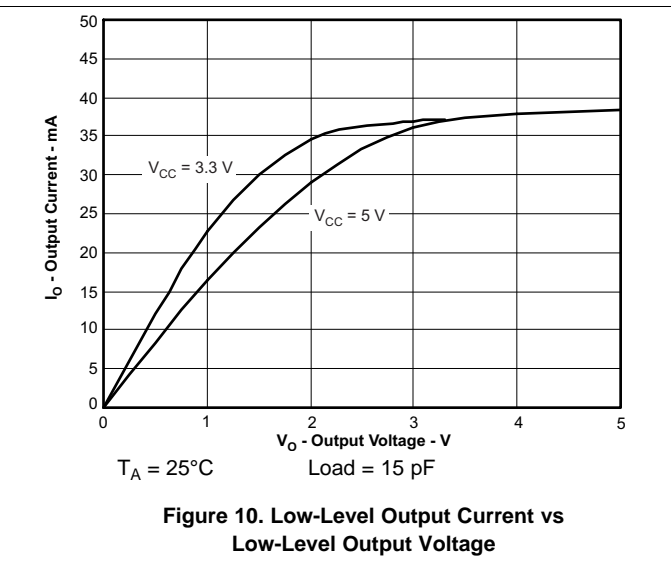
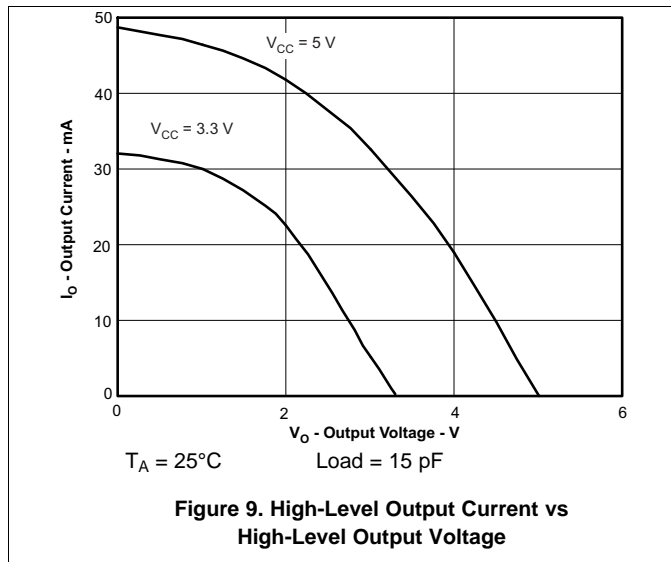
## 7.21 Insulation Characteristics Curves



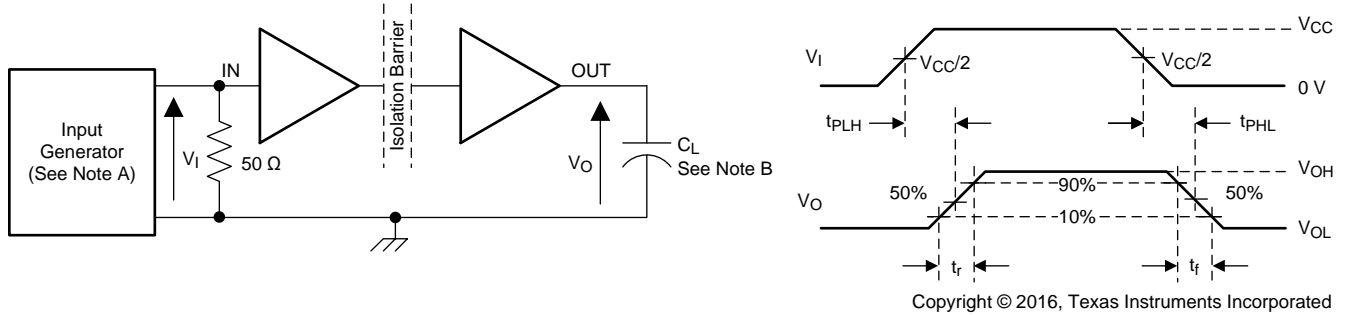
## 7.22 Typical Characteristics



Typical Characteristics (continued)

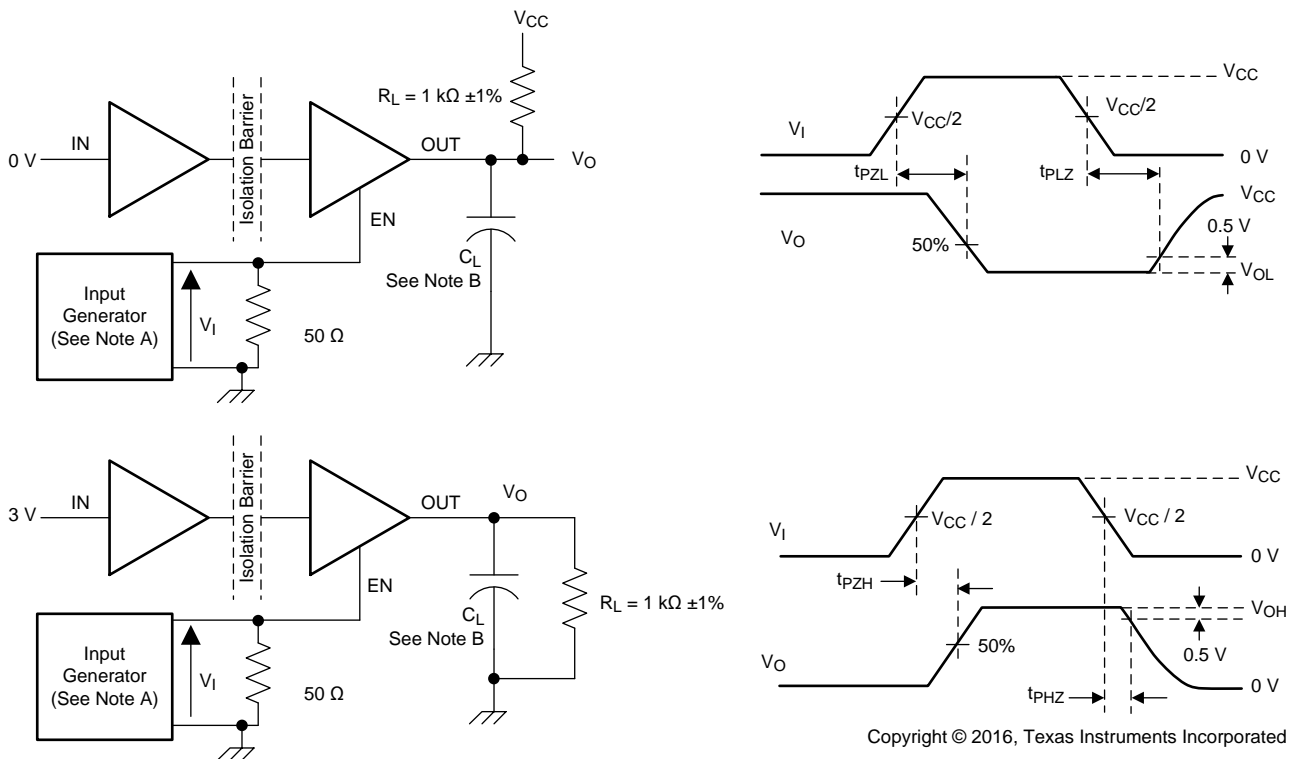


## 8 Parameter Measurement Information



- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50 kHz, 50% duty cycle,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns,  $Z_O = 50 \Omega$ .
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

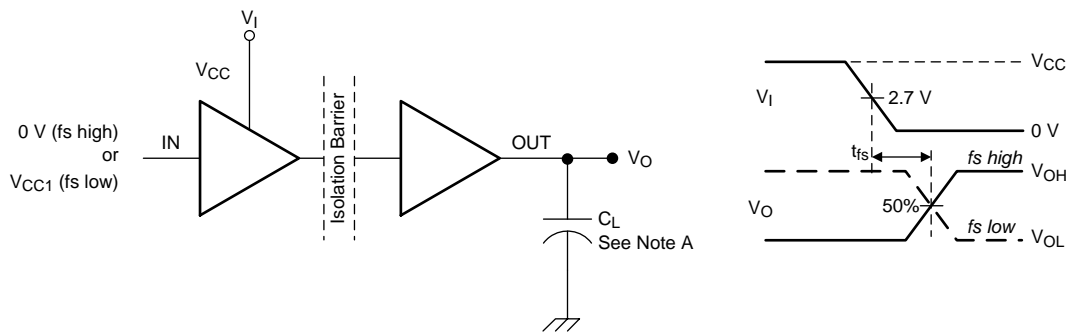
**Figure 11. Switching Characteristic Test Circuit and Voltage Waveforms**



- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50 kHz, 50% duty cycle,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns,  $Z_O = 50 \Omega$ .
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

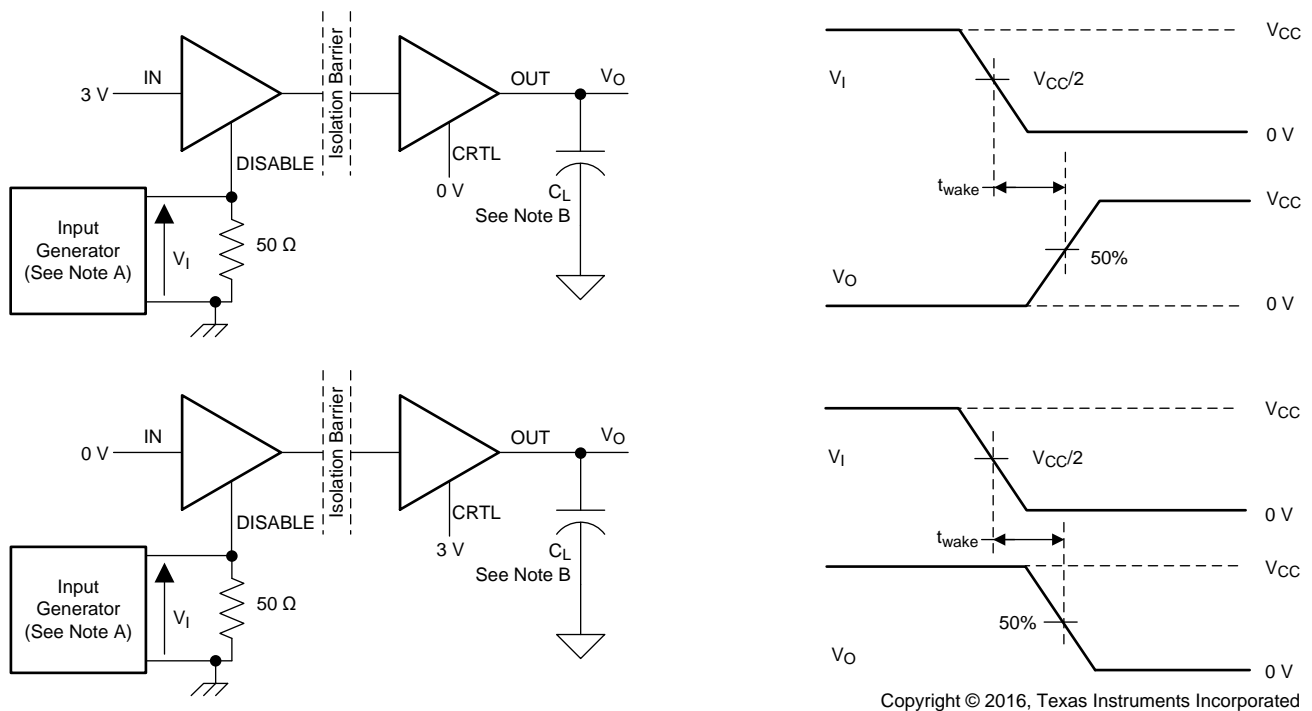
**Figure 12. Enable or Disable Propagation-Delay Time Test Circuit and Waveform**

**Parameter Measurement Information (continued)**



A.  $C_L = 15 \text{ pF}$  and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

**Figure 13. Failsafe Delay Time Test Circuit and Voltage Waveforms**



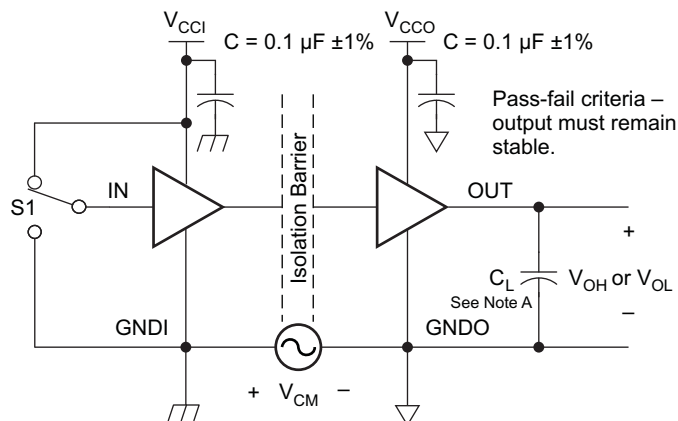
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NOTE: The test that yields the longest time is used in this data sheet.

- A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 50 \text{ kHz}$ , 50% duty cycle,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ ,  $Z_0 = 50 \Omega$ .
- B.  $C_L = 15 \text{ pF}$  and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

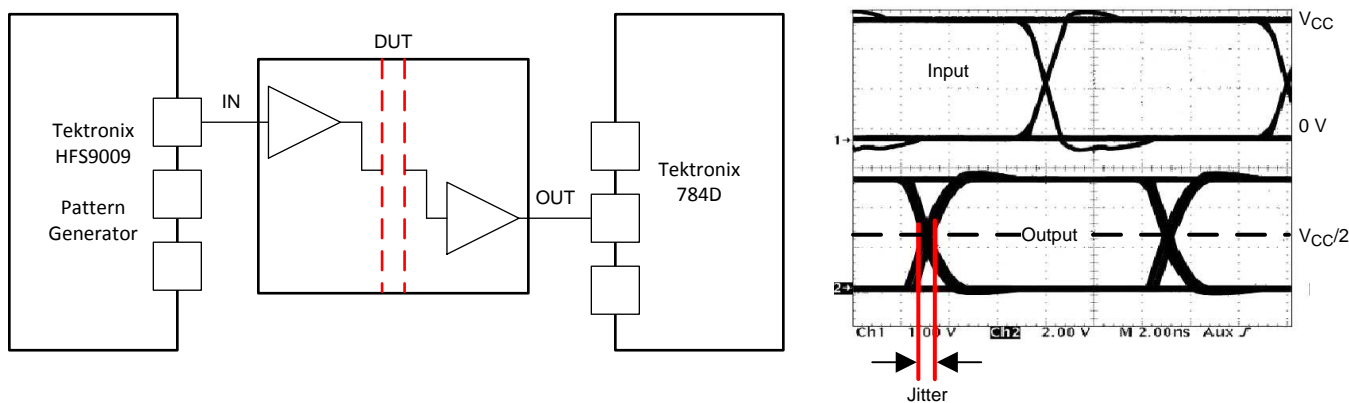
**Figure 14. Wake Time From Input Disable Test Circuit and Voltage Waveforms**

Parameter Measurement Information (continued)



- A.  $C_L = 15 \text{ pF}$  and includes instrumentation and fixture capacitance within  $\pm 20\%$ .
- B. The input pulse is supplied by a generator having the following characteristics:  $\text{PRR} \leq 50 \text{ kHz}$ , 50% duty cycle,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ ,  $Z_0 = 50 \Omega$ .

Figure 15. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



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NOTE: PRBS bit pattern run length is  $2^{16} - 1$ . Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 16. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

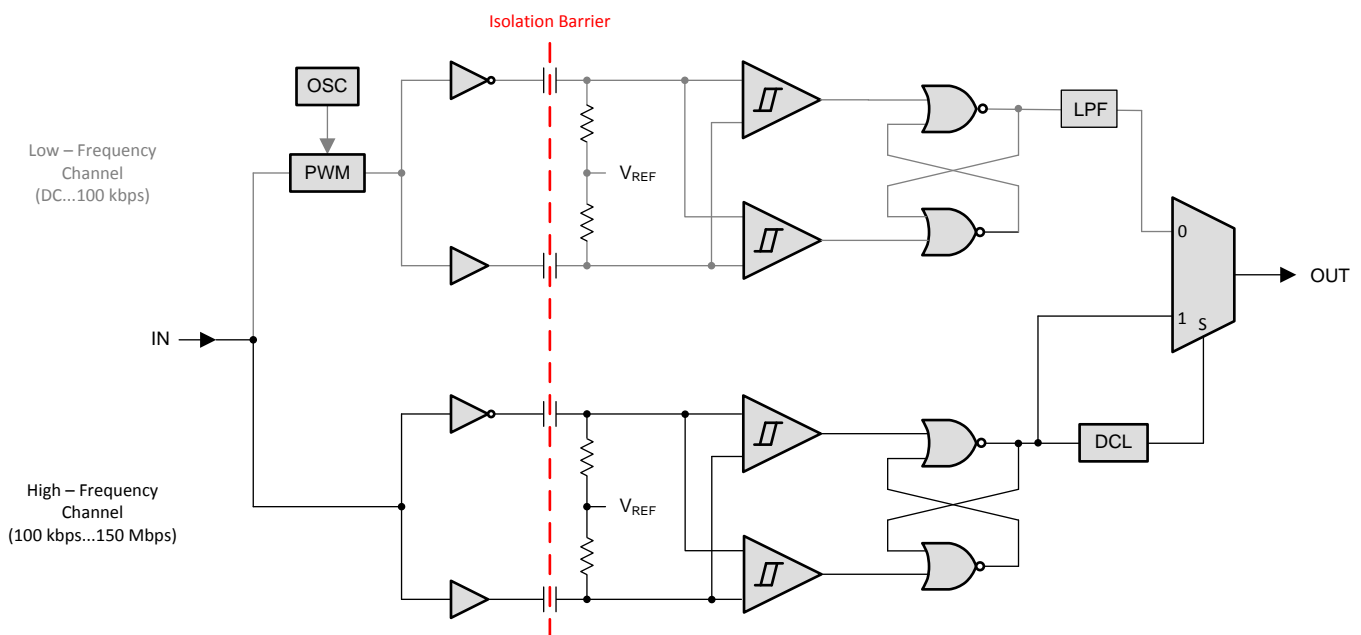
## 9 Detailed Description

### 9.1 Overview

The isolator in Figure 17 is based on a capacitive isolation-barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 150 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single-ended input signal entering the HF-channel is split into a differential signal through the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop the output of which feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, as in the case of a low-frequency signal, the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is required to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

### 9.2 Functional Block Diagram



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Figure 17. Conceptual Block Diagram of a Digital Capacitive Isolator



### 9.3 Feature Description

The ISO724xx family of devices is available in multiple channel configurations and default output-state options to enable wide variety of application uses. [Table 1](#) lists these device features.

**Table 1. Device Features**

| PRODUCT   | SIGNALING RATE | INPUT THRESHOLD   | CHANNEL CONFIGURATION |
|-----------|----------------|-------------------|-----------------------|
| ISO7240C  | 25 Mbps        | ~1.5 V (TTL)      | 4/0                   |
| ISO7240CF | 25 Mbps        | ~1.5 V (TTL)      |                       |
| ISO7240M  | 150 Mbps       | $V_{CC}/2$ (CMOS) |                       |
| ISO7241C  | 25 Mbps        | ~1.5 V (TTL)      | 3/1                   |
| ISO7241M  | 150 Mbps       | $V_{CC}/2$ (CMOS) |                       |
| ISO7242C  | 25 Mbps        | ~1.5 V (TTL)      | 2/2                   |
| ISO7242M  | 150 Mbps       | $V_{CC}/2$ (CMOS) |                       |

### 9.4 Device Functional Modes

[Table 2](#) lists the ISO724xx functional modes. [Table 3](#) lists the ISO7240CF functional modes.

**Table 2. Device Function Table ISO724x<sup>(1)</sup>**

| INPUT $V_{CC}$ | OUTPUT $V_{CC}$ | INPUT (IN) | OUTPUT ENABLE (EN) | OUTPUT (OUT) |
|----------------|-----------------|------------|--------------------|--------------|
| PU             | PU              | H          | H or Open          | H            |
|                |                 | L          | H or Open          | L            |
|                |                 | X          | L                  | Z            |
|                |                 | Open       | H or Open          | H            |
| PD             | PU              | X          | H or Open          | H            |
| PD             | PU              | X          | L                  | Z            |
| X              | PD              | X          | X                  | Undetermined |

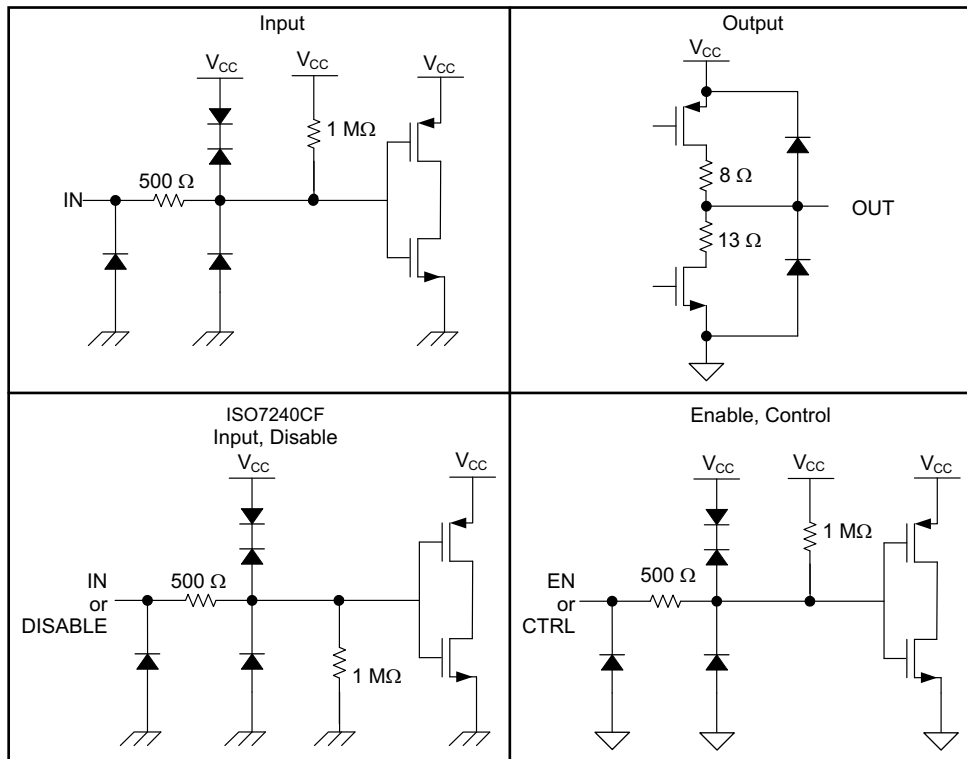
(1) PU = Powered Up; PD = Powered Down; X = Irrelevant; H = High Level; L = Low Level; Z = High Impedance; Open = Not Connected

**Table 3. ISO7240CF Functions Table<sup>(1)</sup>**

| $V_{CC1}$ | $V_{CC2}$ | DATA INPUT (IN) | DISABLE INPUT (DISABLE) | FAILSAFE CONTROL (CTRL) | DATA OUTPUT (OUT) |
|-----------|-----------|-----------------|-------------------------|-------------------------|-------------------|
| PU        | PU        | H               | L or Open               | X                       | H                 |
| PU        | PU        | L               | L or Open               | X                       | L                 |
| X         | PU        | X               | H                       | H or Open               | H                 |
| X         | PU        | X               | H                       | L                       | L                 |
| PD        | PU        | X               | X                       | H or Open               | H                 |
| PD        | PU        | X               | X                       | L                       | L                 |
| X         | PD        | X               | X                       | X                       | Undetermined      |

(1) PU = Powered Up; PD = Powered Down; X = Irrelevant; H = High Level; L = Low Level; Z = High Impedance; Open = Not Connected

9.4.1 Device I/O Schematics



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Figure 18. Device I/O Schematics

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

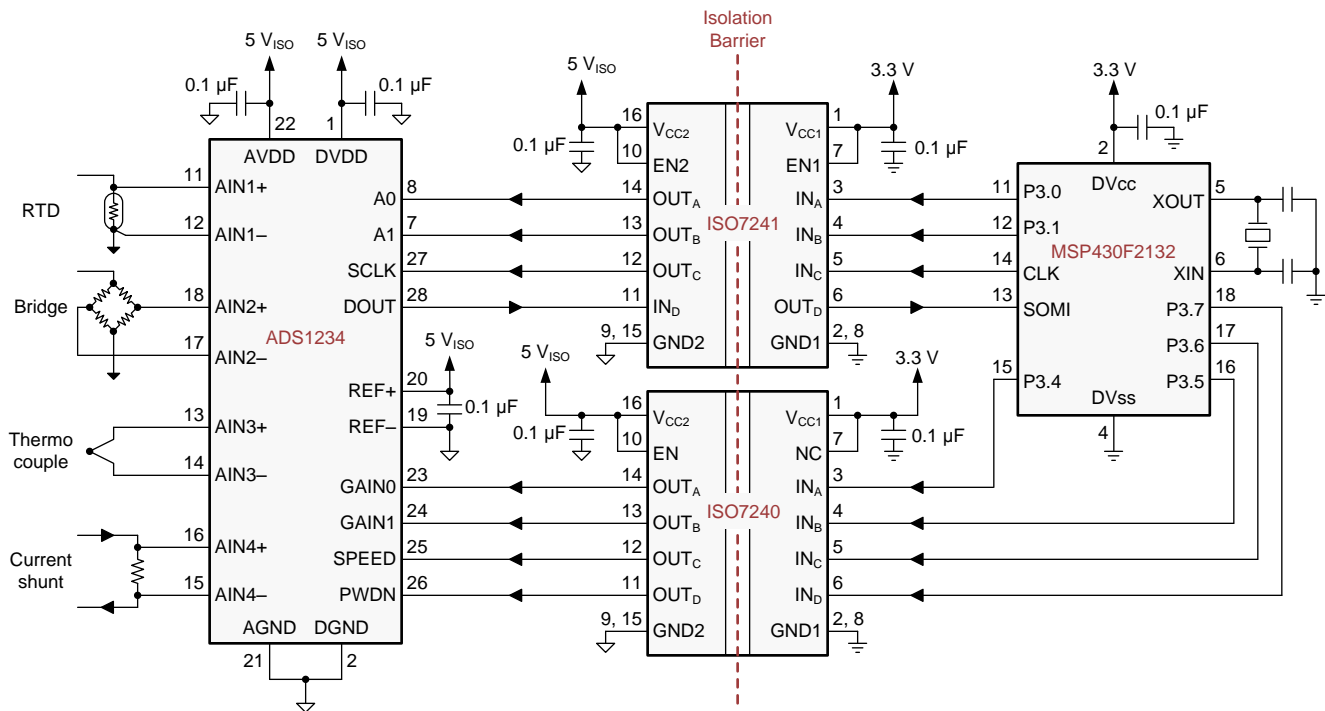
### 10.1 Application Information

The ISO724xx family of devices uses a single-ended TTL or CMOS-logic switching technology. The supply voltage range is from 3.15 V to 5.5 V for both supplies,  $V_{CC1}$  and  $V_{CC2}$ . When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is,  $\mu$ C or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

### 10.2 Typical Application

#### 10.2.1 Isolated Data Acquisition System for Process Control

The ISO724xx family of devices can be used with Texas Instruments' precision analog-to-digital converter and mixed signal microcontroller to create an advanced isolated data acquisition system as shown in Figure 19.



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Figure 19. Isolated Data Acquisition System for Process Control

#### 10.2.1.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO724x family of devices only require two external bypass capacitors to operate.

Typical Application (continued)

10.2.1.2 Detailed Design Procedure

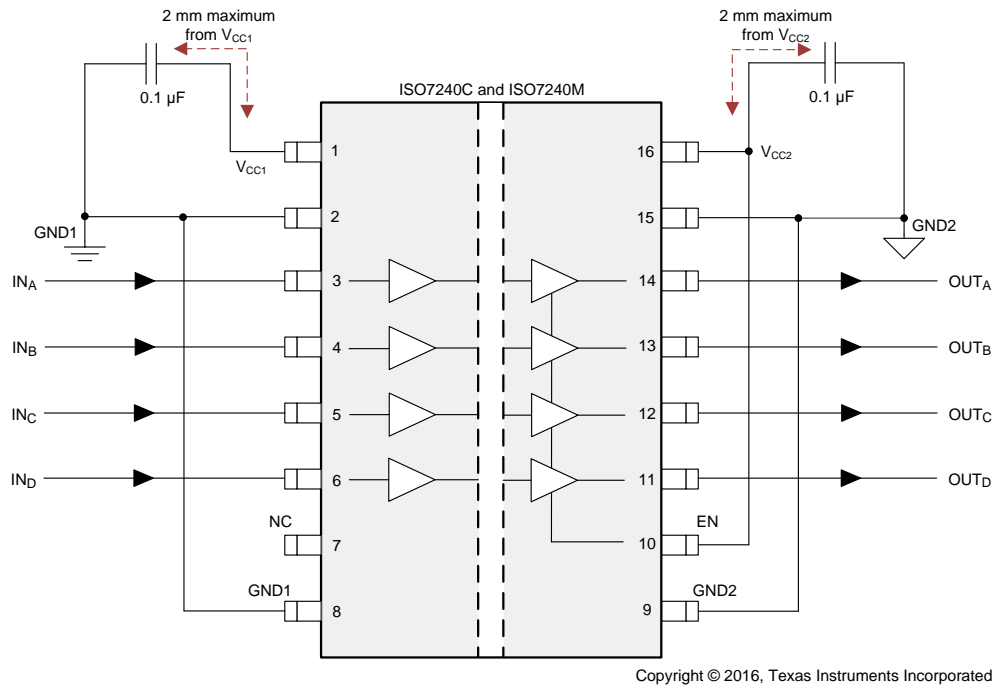


Figure 20. ISO7240x Typical Circuit Hook-Up

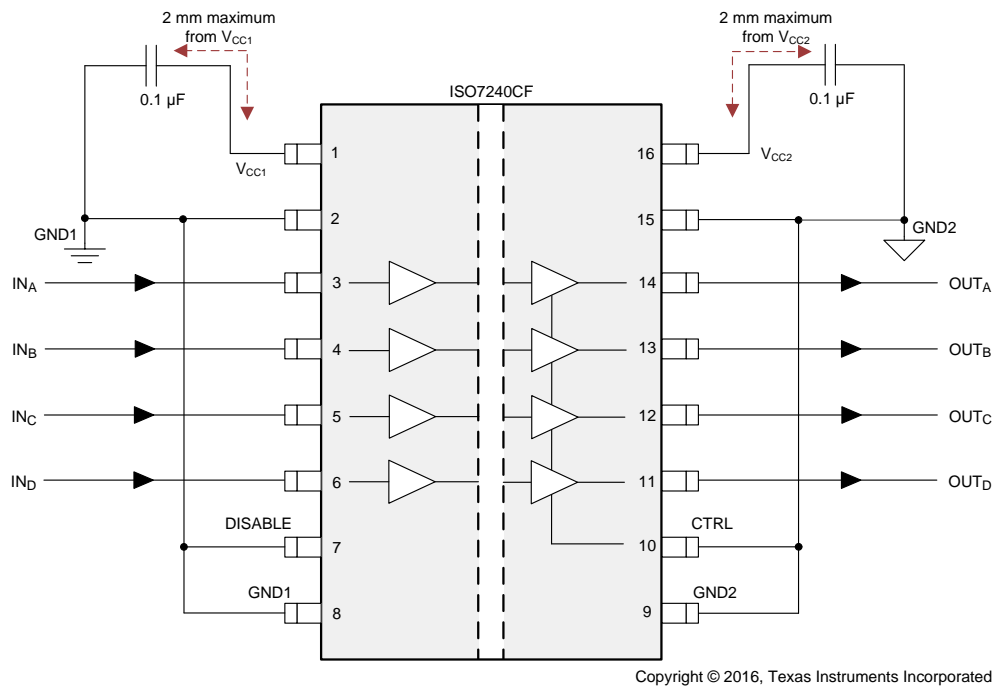


Figure 21. ISO7240CF Typical Circuit Hook-Up

Typical Application (continued)

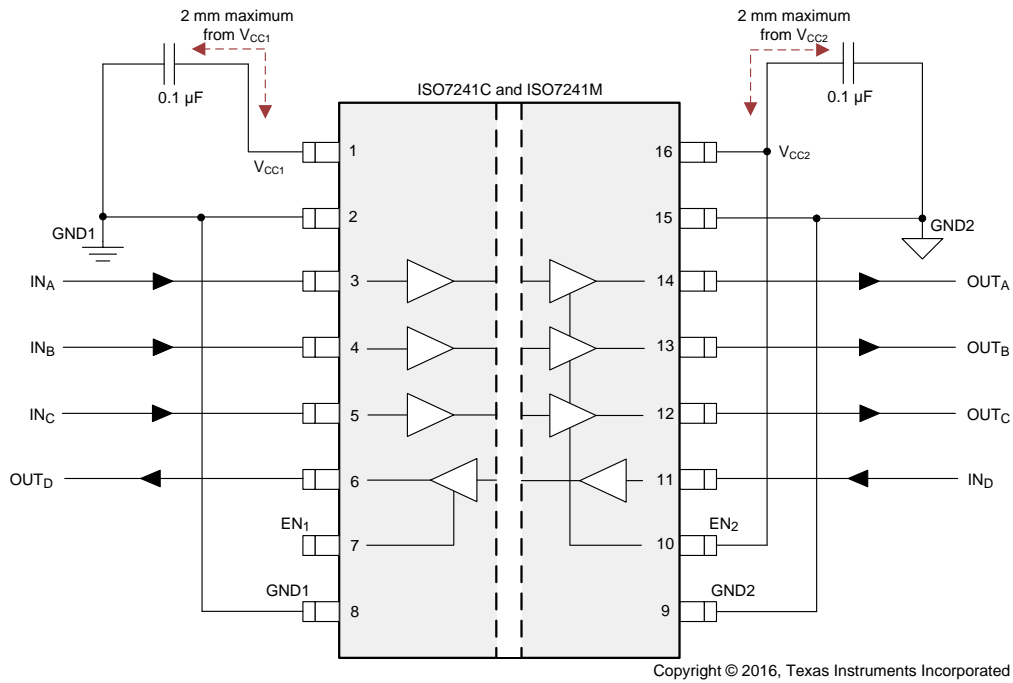


Figure 22. ISO7241x Typical Circuit Hook-Up

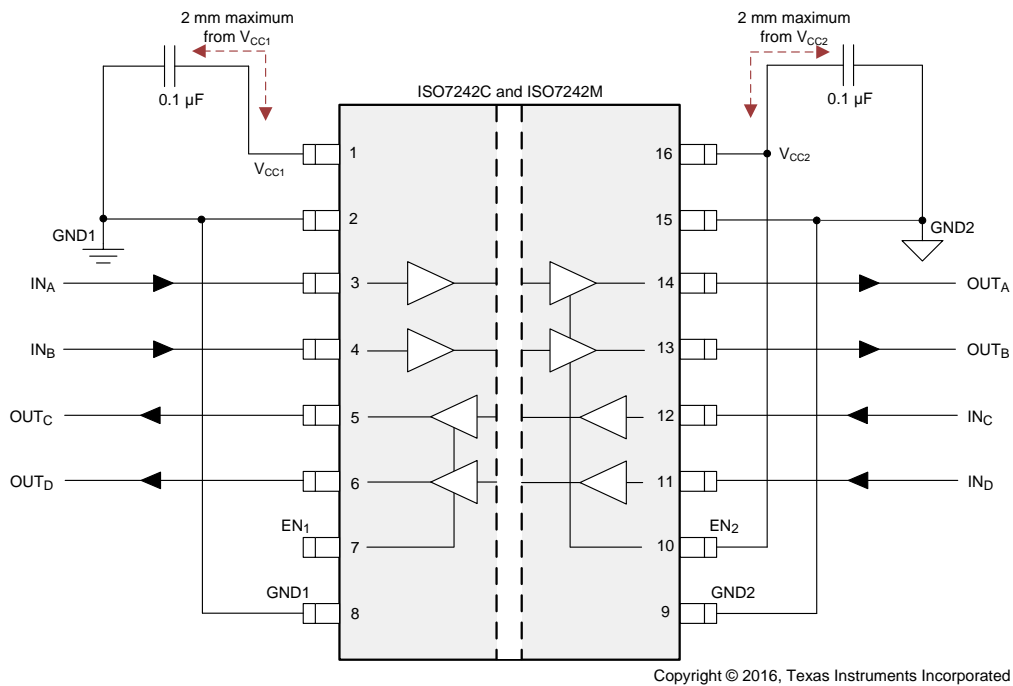


Figure 23. ISO7242x Typical Circuit Hook-Up

## Typical Application (continued)

### 10.2.1.3 Application Curves

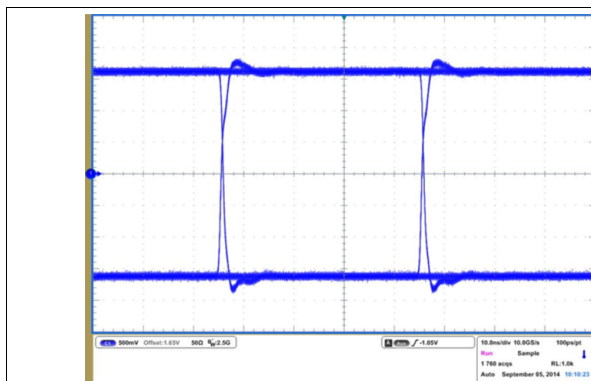


Figure 24. ISO7242M Eye Diagram at 25 Mbps, 3.3 V and 25°C

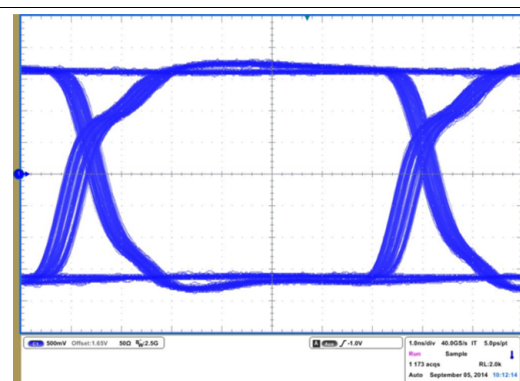
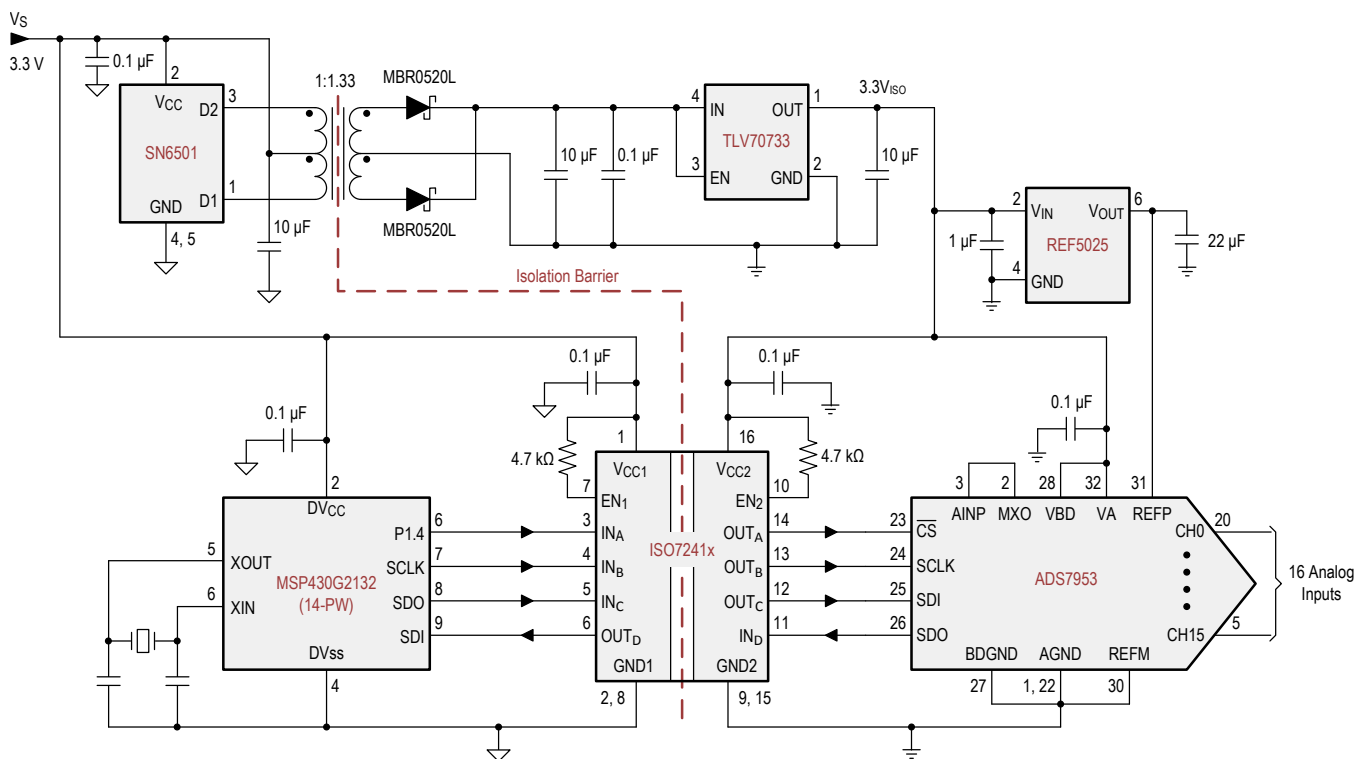


Figure 25. ISO7242M Eye Diagram at 150 Mbps, 3.3 V and 25°C

### 10.2.2 Isolated SPI for an Analog Input Module with 16 Inputs

The ISO7241x family of devices and several other components from Texas Instruments can be used to create an isolated SPI for an input module with 16 inputs.



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Figure 26. Isolated SPI for an Analog Input Module With 16 Inputs

#### 10.2.2.1 Design Requirements

See the [Design Requirements](#) in the [Isolated Data Acquisition System for Process Control](#) section.

## Typical Application (continued)

### 10.2.2.2 Detailed Design Procedure

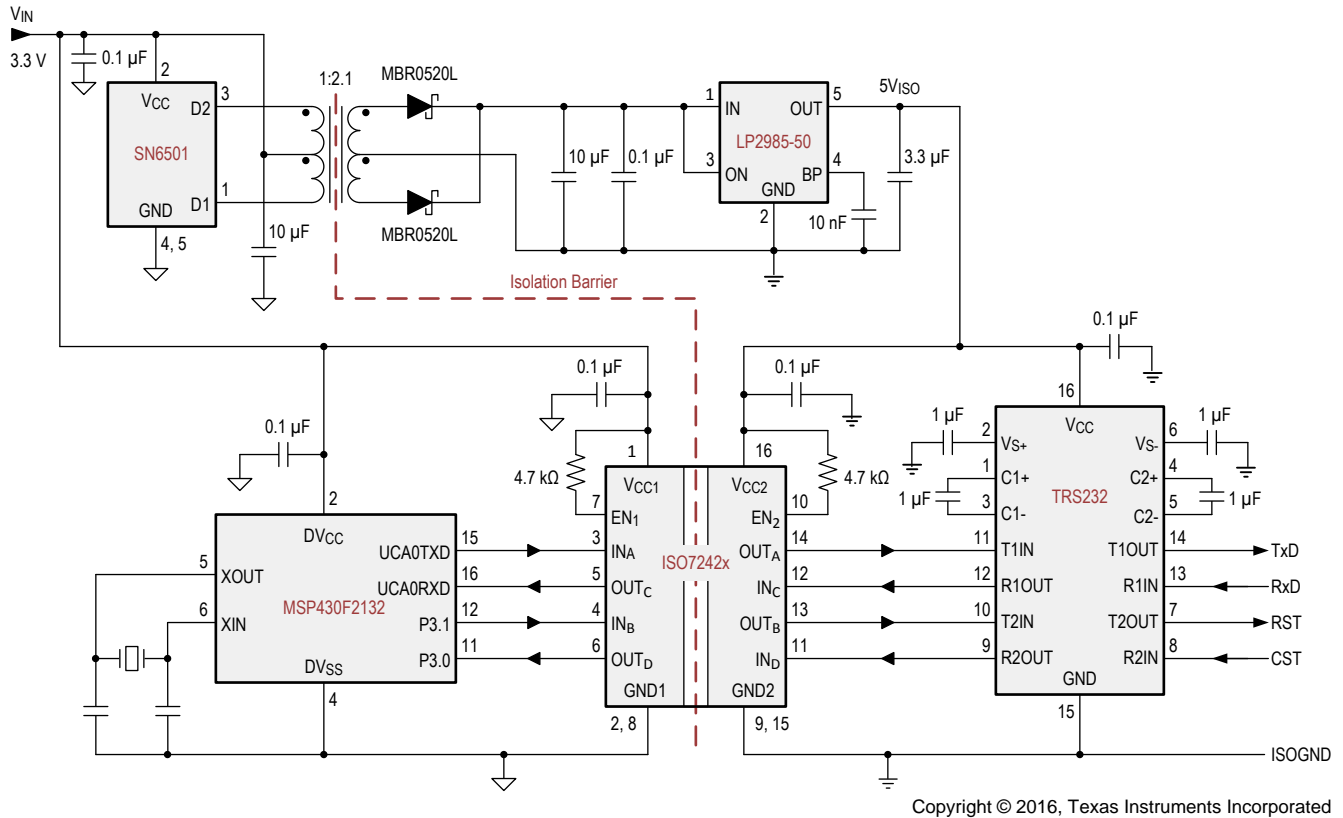
See the [Detailed Design Procedure](#) in the *Isolated Data Acquisition System for Process Control* section..

### 10.2.2.3 Application Curve

See the [Application Curves](#) in the *Isolated Data Acquisition System for Process Control* section..

## 10.2.3 Isolated RS-232 Interface

Figure 27 shows a typical isolated RS-232 interface implementation.



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Figure 27. Isolated RS-232 Interface

### 10.2.3.1 Design Requirements

See the [Design Requirements](#) in the *Isolated Data Acquisition System for Process Control* section.

### 10.2.3.2 Detailed Design Procedure

See the [Detailed Design Procedure](#) in the *Isolated Data Acquisition System for Process Control* section..

### 10.2.3.3 Application Curve

See the [Application Curves](#) in the *Isolated Data Acquisition System for Process Control* section..

## 11 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1- $\mu$ F bypass capacitor is recommended at input and output supply pins (VCC1 and VCC2). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' [SN6501](#) device. For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501 Transformer Driver for Isolated Power Supplies](#).

## 12 Layout

### 12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 28](#)). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in<sup>2</sup>.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to [Digital Isolator Design Guide](#).

#### 12.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

### 12.2 Layout Example

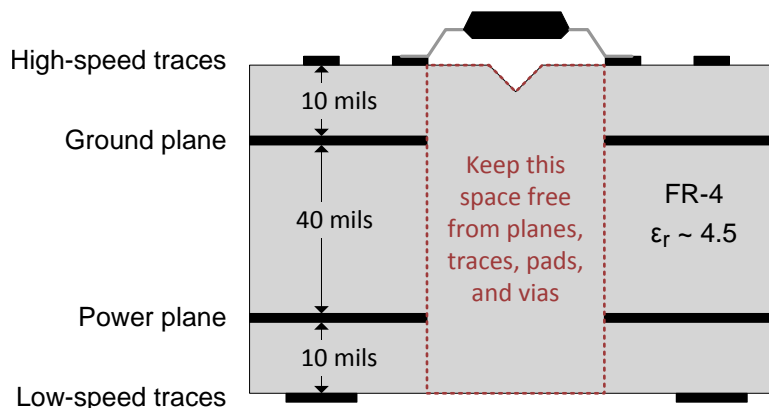


Figure 28. Recommended Layer Stack



## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation, see the following:

- [ADS1234 24-Bit Analog-to-Digital Converter For Bridge Sensors](#)
- [ADS79xx 12/10/8-Bit, 1 MSPS, 16/12/8/4-Channel, Single-Ended, MicroPower, Serial Interface ADCs](#)
- [Digital Isolator Design Guide](#)
- [High-Voltage Lifetime of the ISO72x Family of Digital Isolators](#)
- [ISO72x Digital Isolator Magnetic-Field Immunity](#)
- [Isolation Glossary](#)
- [LP2985 150-mA Low-noise Low-dropout Regulator With Shutdown](#)
- [MSP430F2132 Mixed Signal Microcontroller](#)
- [MSP430G2x32, MSP430G2x02 Mixed Signal Microcontroller](#)
- [REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference](#)
- [SN6501 Transformer Driver for Isolated Power Supplies](#)
- [TLV707, TLV707P 200-mA, Low-IQ, Low-Noise, Low-Dropout Regulator for Portable Devices](#)
- [TRS232 Dual RS-232 Driver/Receiver With IEC61000-4-2 Protection](#)

### 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 4. Related Links**

| PARTS     | PRODUCT FOLDER             | ORDER NOW                  | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| ISO7240CF | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| ISO7240C  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| ISO7240M  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| ISO7241C  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| ISO7241M  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| ISO7242C  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| ISO7242M  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.5 Trademarks

### 13.5 Trademarks (continued)

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| ISO7240CDW       | LIFEBUY       | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7240C                |         |
| ISO7240CDWG4     | LIFEBUY       | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7240C                |         |
| ISO7240CDWR      | ACTIVE        | SOIC         | DW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7240C                | Samples |
| ISO7240CFDW      | LIFEBUY       | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7240CF               |         |
| ISO7240CFDWG4    | LIFEBUY       | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7240CF               |         |
| ISO7240CFDWR     | ACTIVE        | SOIC         | DW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7240CF               | Samples |
| ISO7240MDW       | LIFEBUY       | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7240M                |         |
| ISO7240MDWG4     | LIFEBUY       | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7240M                |         |
| ISO7240MDWR      | ACTIVE        | SOIC         | DW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7240M                | Samples |
| ISO7240MDWRG4    | ACTIVE        | SOIC         | DW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7240M                | Samples |
| ISO7241CDW       | LIFEBUY       | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7241C                |         |
| ISO7241CDWG4     | LIFEBUY       | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7241C                |         |
| ISO7241CDWR      | ACTIVE        | SOIC         | DW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7241C                | Samples |
| ISO7241CDWRG4    | ACTIVE        | SOIC         | DW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7241C                | Samples |
| ISO7241MDW       | LIFEBUY       | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7241M                |         |
| ISO7241MDWG4     | LIFEBUY       | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7241M                |         |
| ISO7241MDWR      | ACTIVE        | SOIC         | DW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7241M                | Samples |
| ISO7241MDWRG4    | ACTIVE        | SOIC         | DW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7241M                | Samples |
| ISO7242CDW       | LIFEBUY       | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7242C                |         |
| ISO7242CDWG4     | LIFEBUY       | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7242C                |         |
| ISO7242CDWR      | ACTIVE        | SOIC         | DW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7242C                | Samples |
| ISO7242MDW       | LIFEBUY       | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7242M                |         |
| ISO7242MDWG4     | LIFEBUY       | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7242M                |         |
| ISO7242MDWR      | ACTIVE        | SOIC         | DW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7242M                | Samples |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| ISO7242MDWRG4    | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO7242M                | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF ISO7240CF, ISO7241C, ISO7242C :**

- Automotive : [ISO7240CF-Q1](#), [ISO7241C-Q1](#), [ISO7242C-Q1](#)

**NOTE: Qualified Version Definitions:**

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

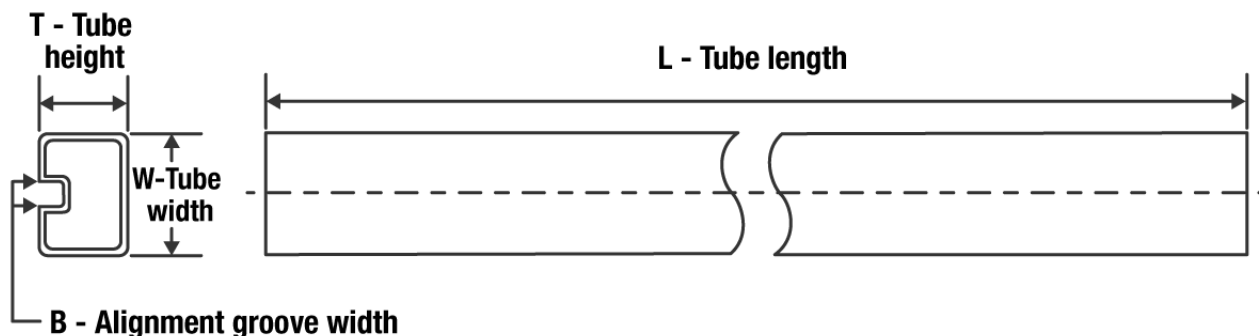

\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ISO7240CDWR  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO7240CFDWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO7240MDWR  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO7241CDWR  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO7241MDWR  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO7242CDWR  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO7242MDWR  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ISO7240CDWR  | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| ISO7240CFDWR | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| ISO7240MDWR  | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| ISO7241CDWR  | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| ISO7241MDWR  | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| ISO7242CDWR  | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| ISO7242MDWR  | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |

**TUBE**


\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| ISO7240CDW    | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO7240CDWG4  | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO7240CFDW   | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO7240CFDWG4 | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO7240MDW    | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO7240MDWG4  | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO7241CDW    | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO7241CDWG4  | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO7241MDW    | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO7241MDWG4  | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO7242CDW    | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO7242CDWG4  | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO7242MDW    | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO7242MDWG4  | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |



## GENERIC PACKAGE VIEW

**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

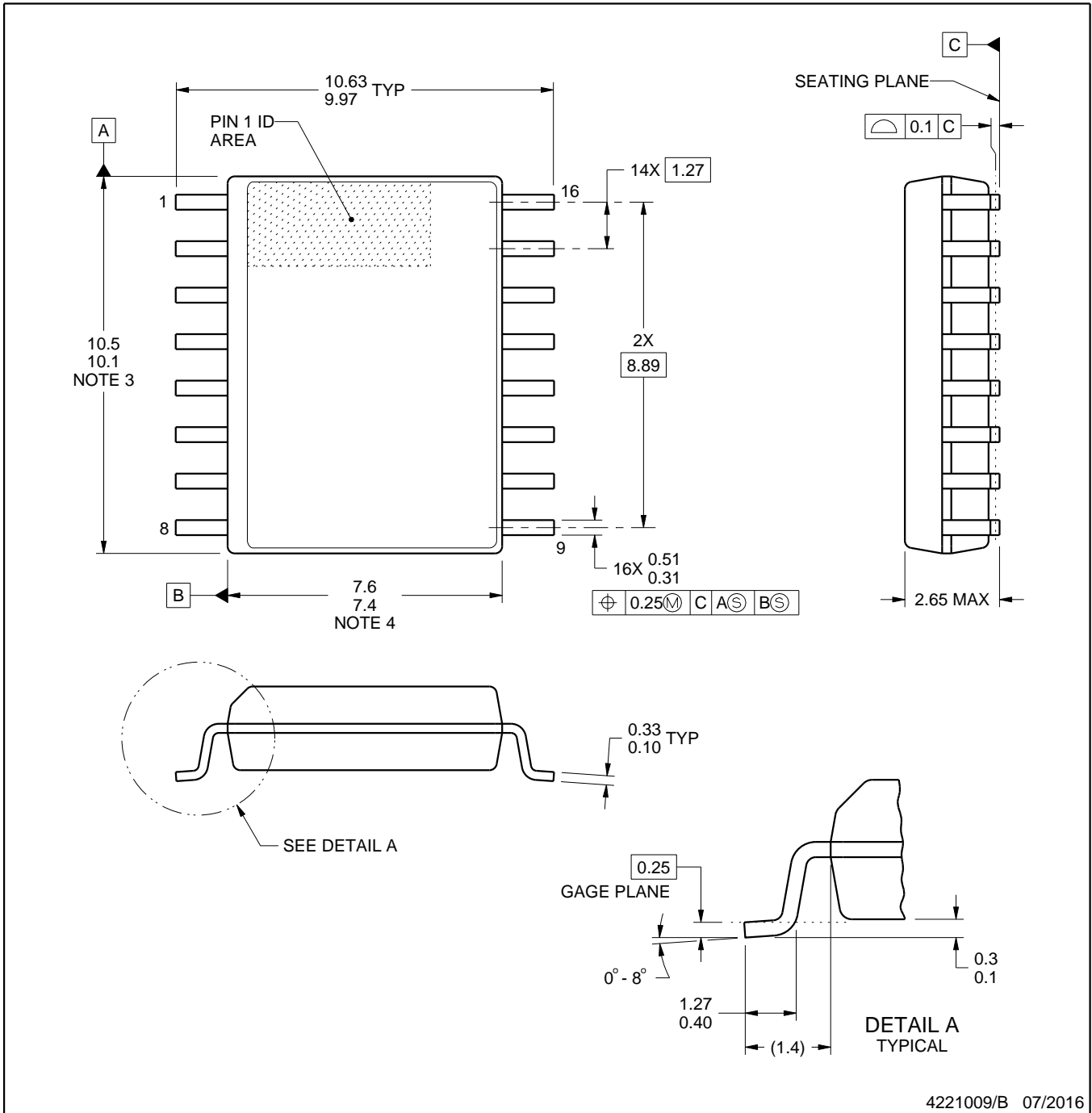


DW0016B

# PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

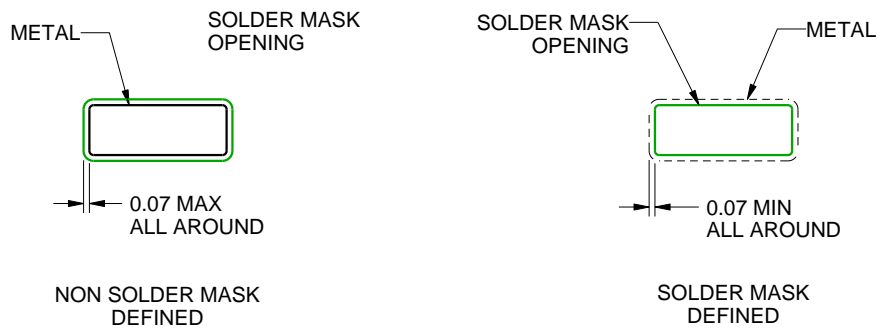
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

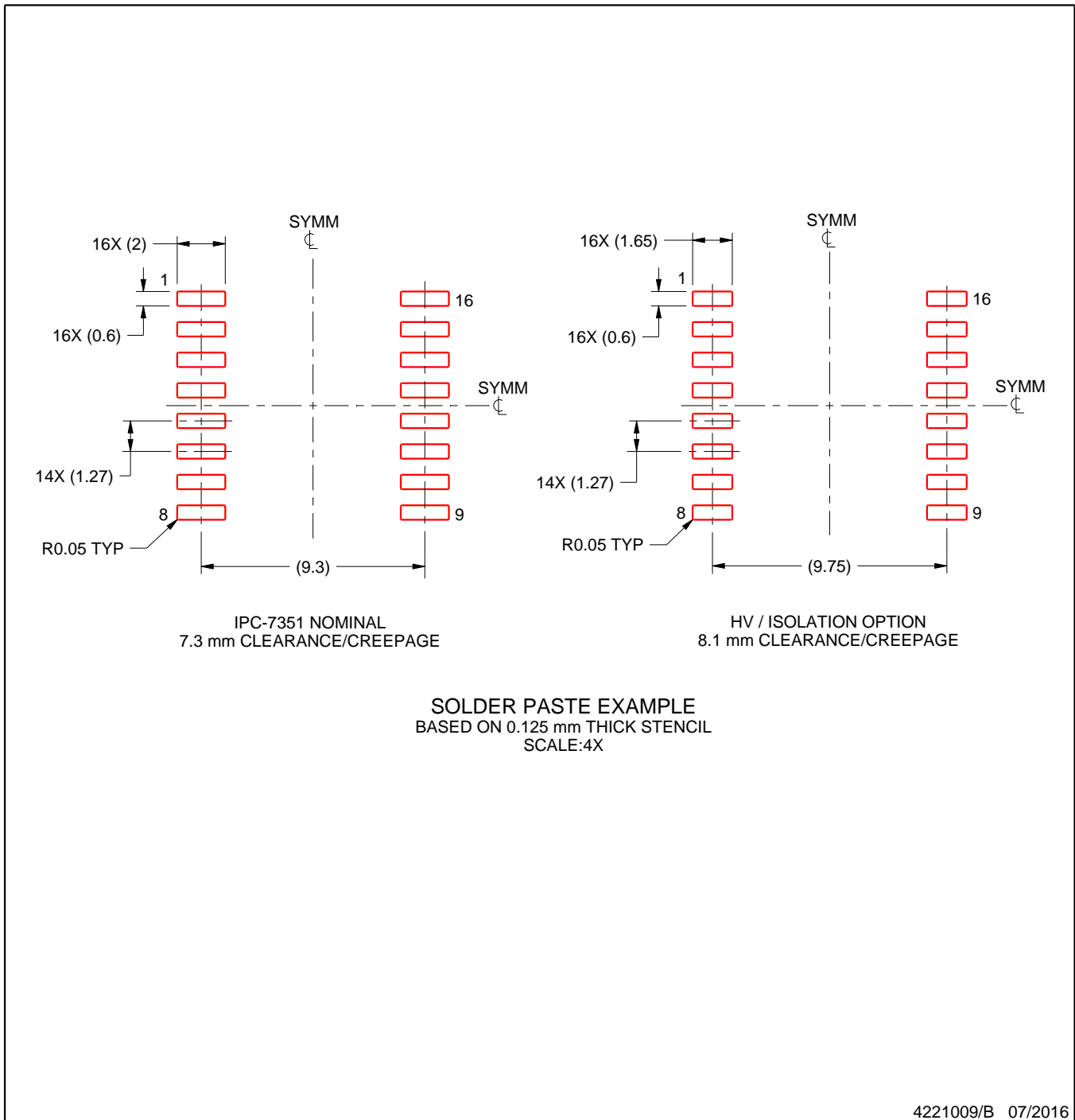
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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